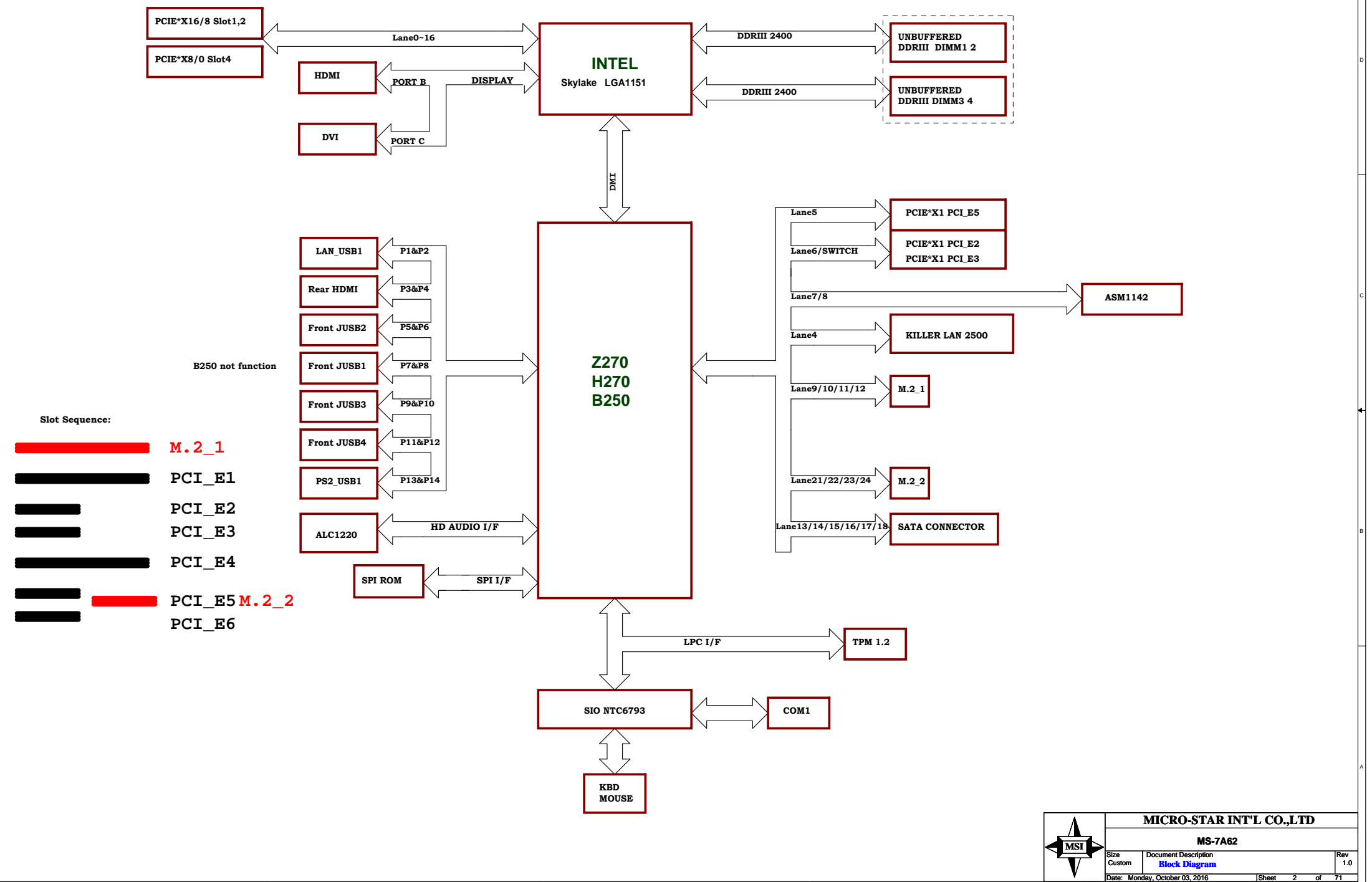
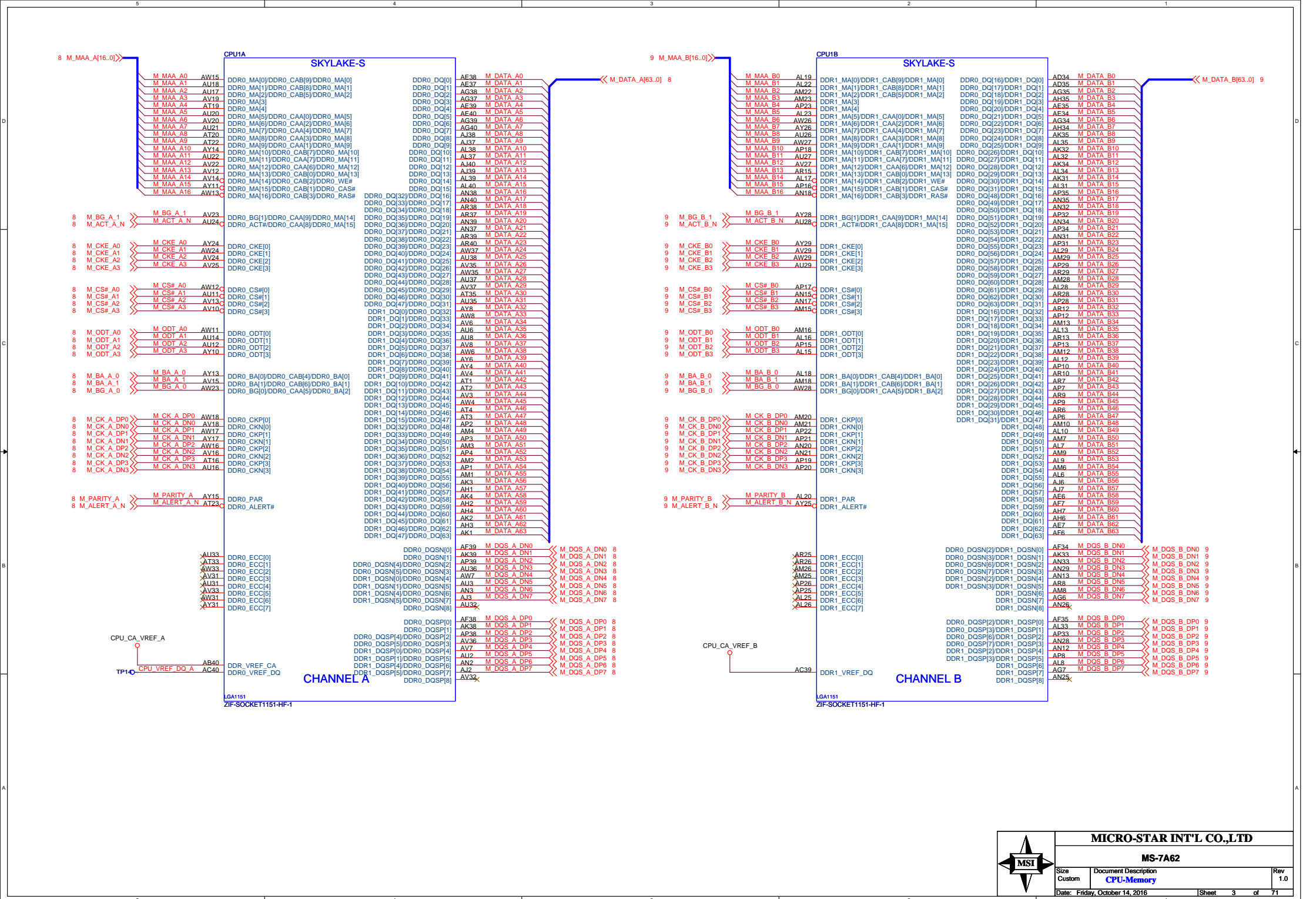
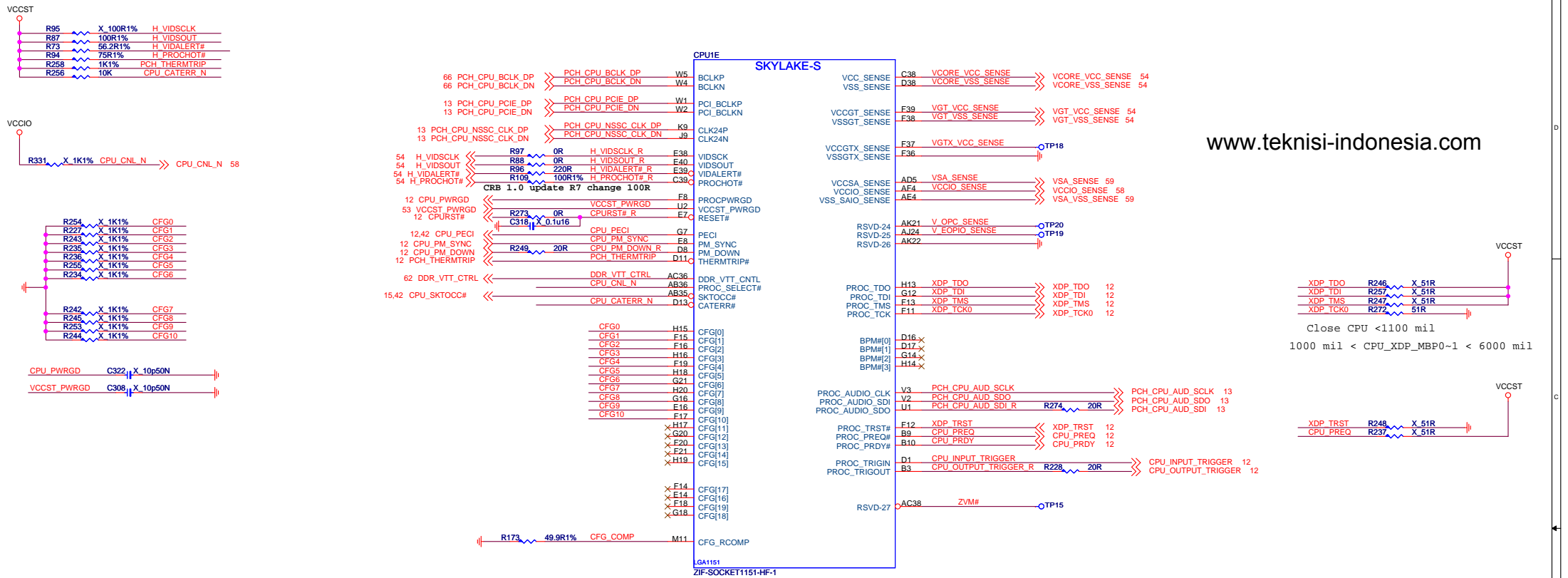




MS-7A62 Block Diagram

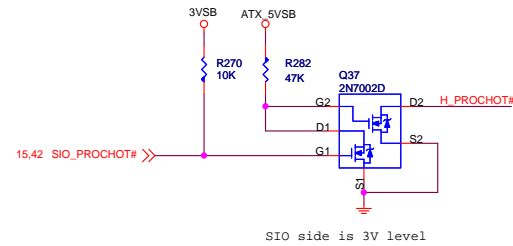






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Close CPU <1100 mil  
1000 mil < CPU\_XDP\_MBP0~1 < 6000 mil



### CFG Strap

CFG Table

HIGH	LOW	DESCRIPTION
0	No Lock	Lock
1	No Lock	Lock
2	NORM	REVERSE
3	DISABLE	ENABLE
4	DISABLE	ENABLE
5	DISABLE	ENABLE
6	DISABLE	ENABLE
7	RESET#	BIOS REQ
8	PRESENT	NO PRESENT
9	PRESENT	NO PRESENT
10	RSVD	RSVD
11	RSVD	RSVD
12	RSVD	RSVD
13	RSVD	RSVD
14	RSVD	RSVD
15	RSVD	RSVD

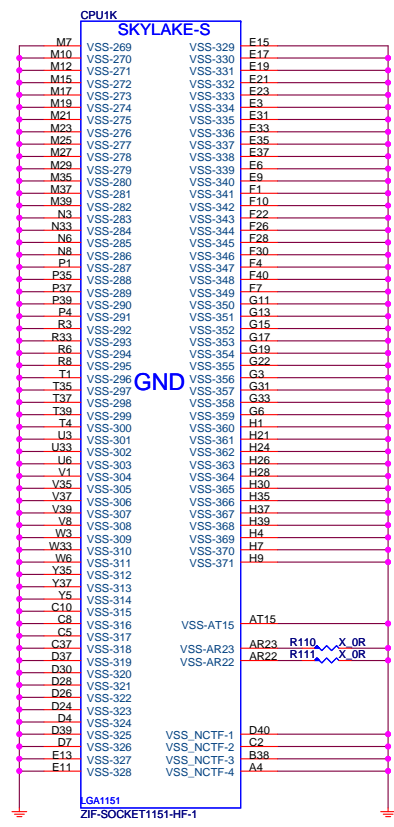
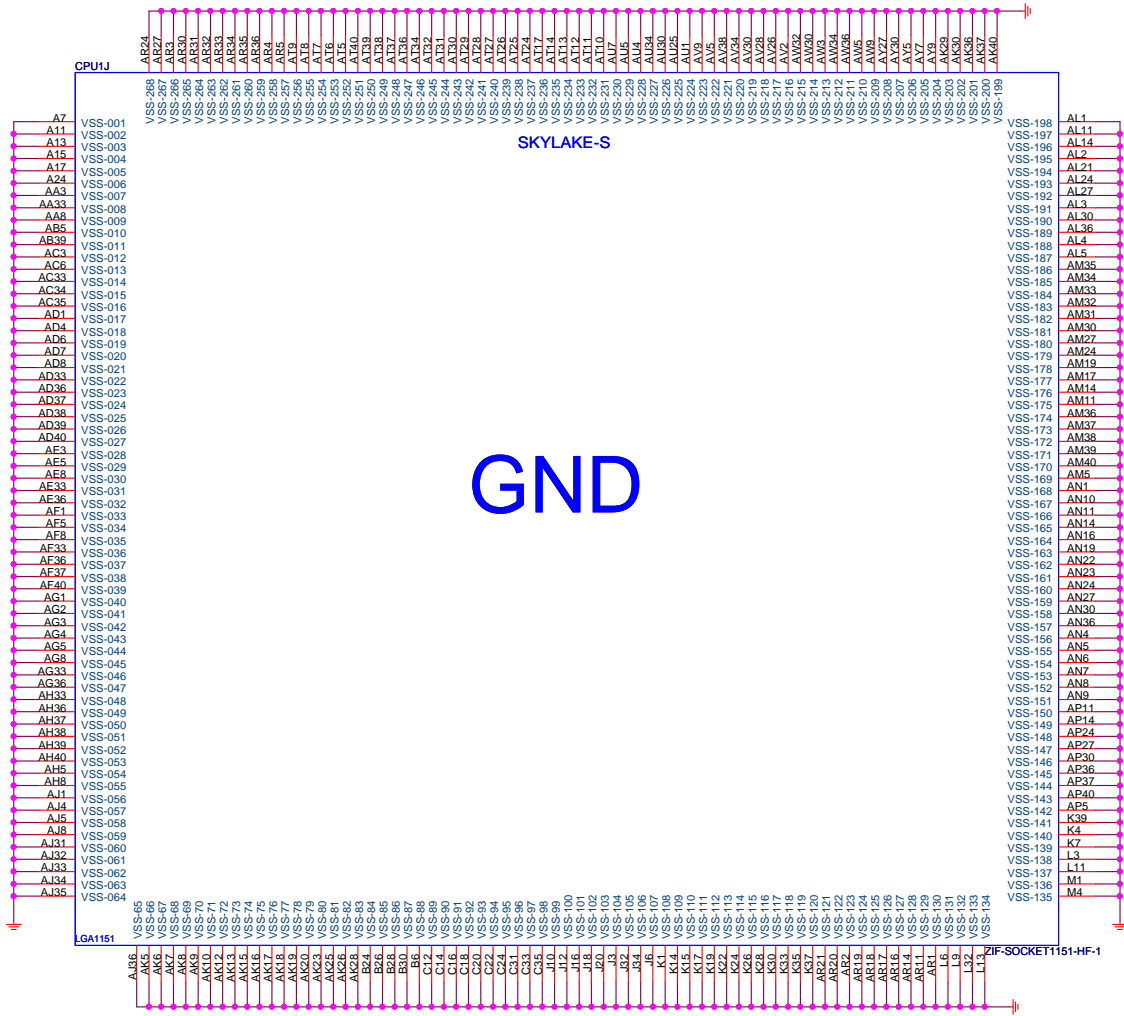
**MICRO-STAR INT'L CO.,LTD**

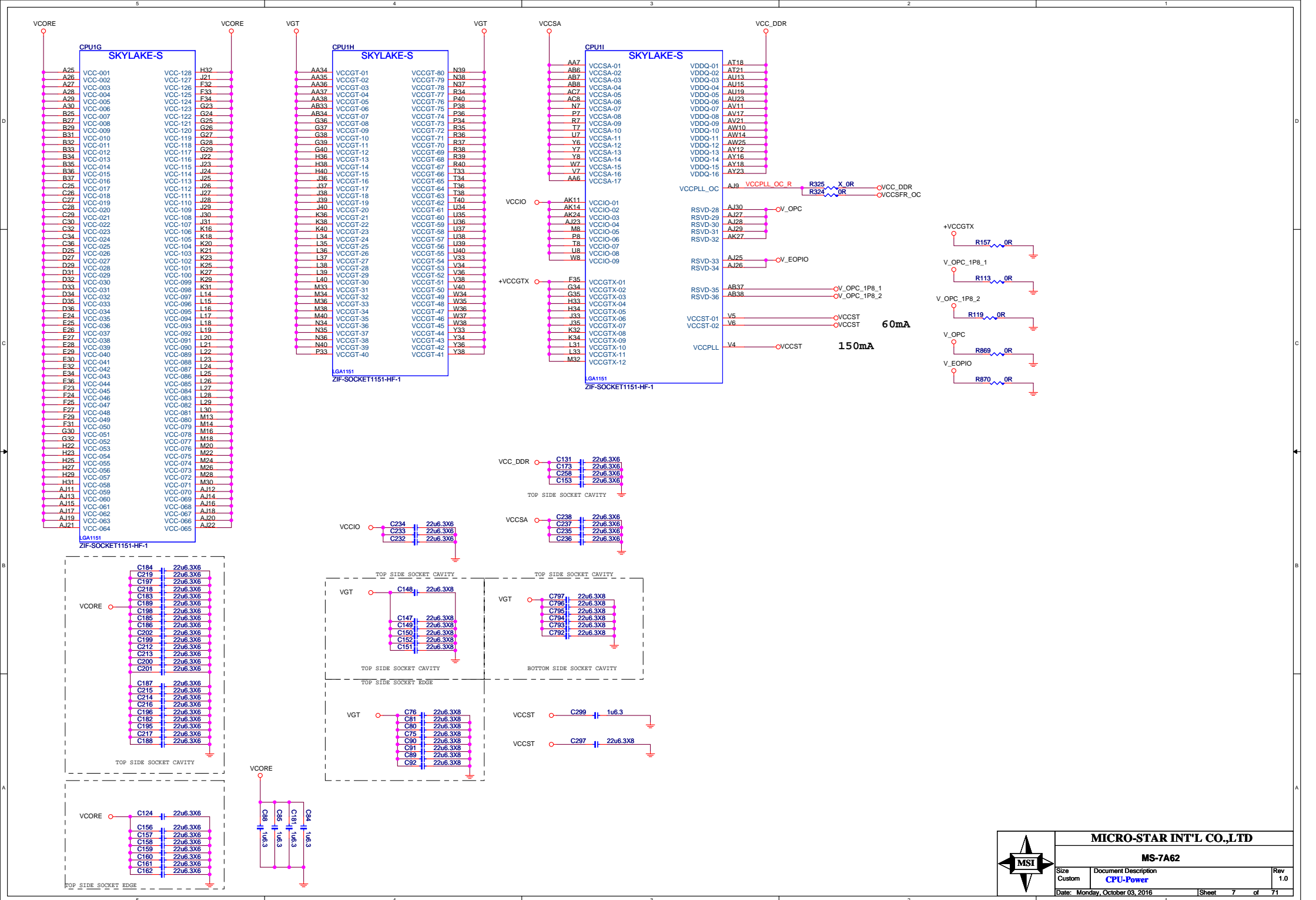
**MS-7A62**

Size Custom | Document Description CPU-Control/MISC/CFG/Audio | Rev 1.0

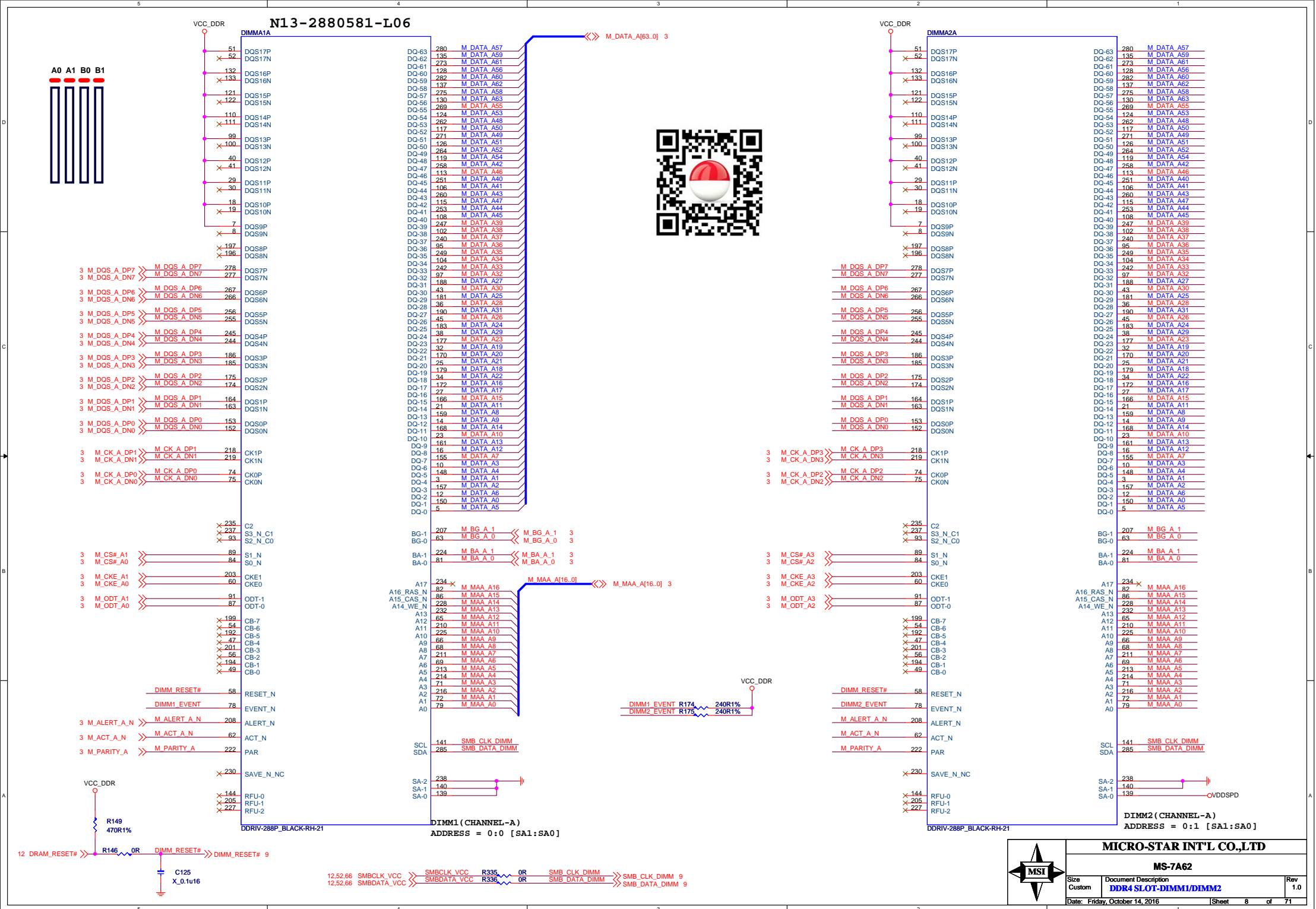
Date: Friday, October 14, 2016 | Sheet 4 of 71



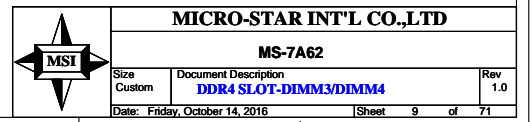


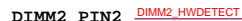
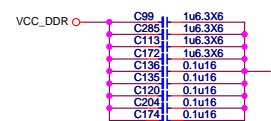
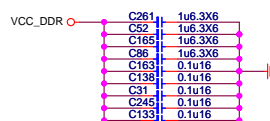
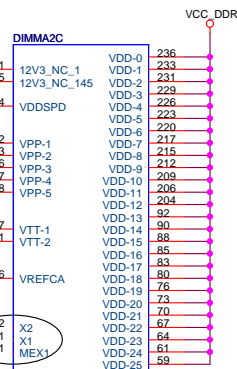
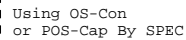
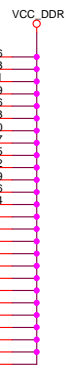




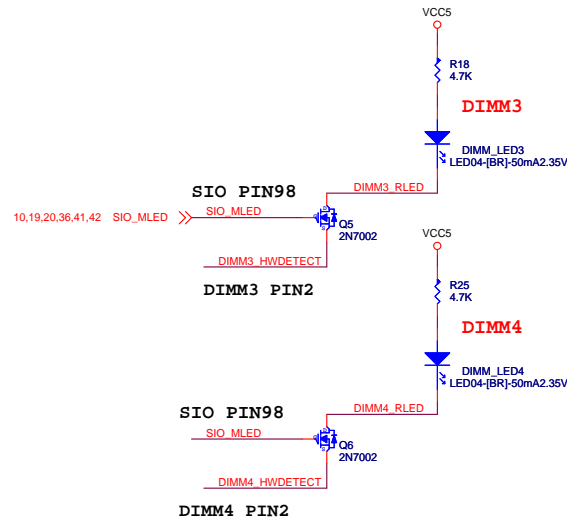
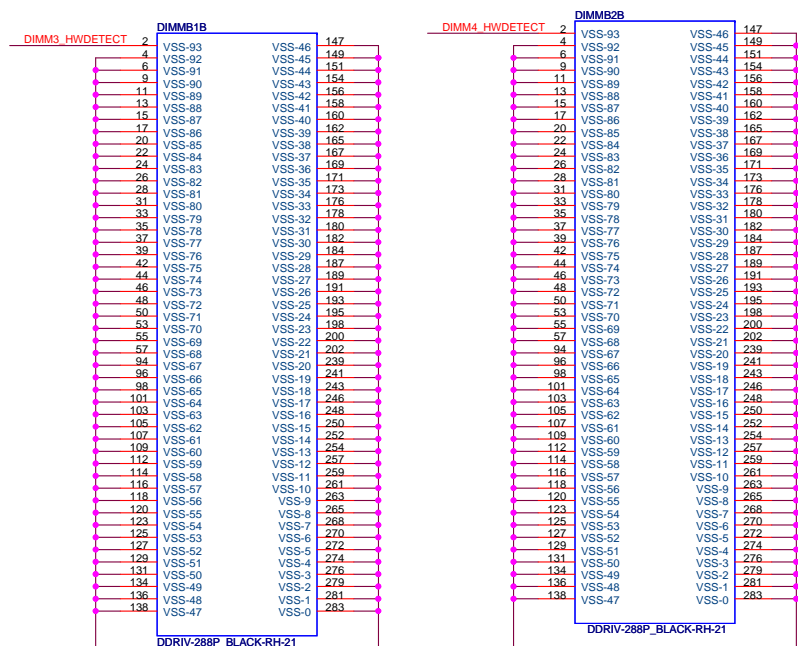
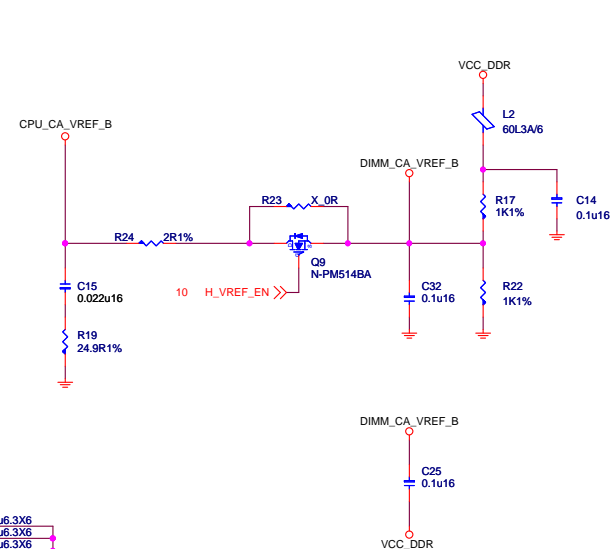
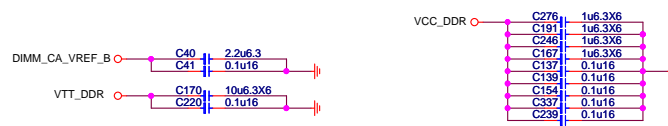
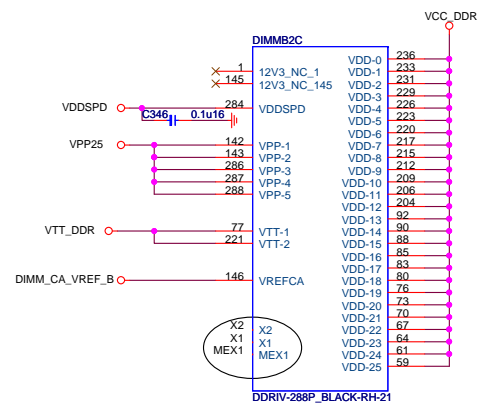
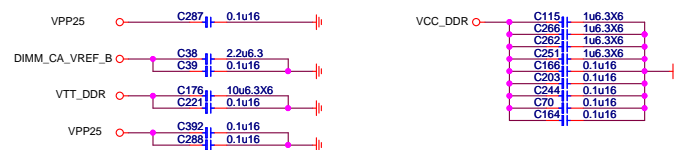
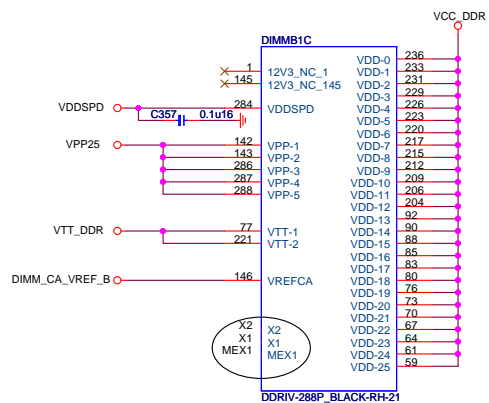




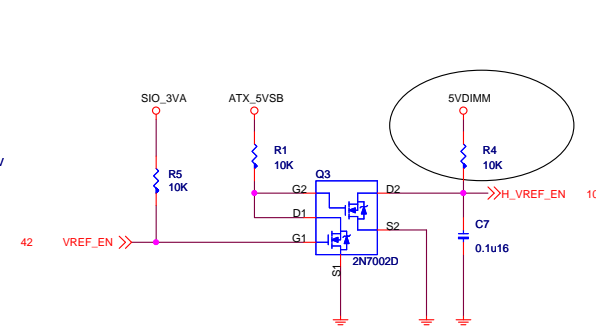




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LED  
RED:D0C-040P100-H91  
AVL:D0C-040S500-E07

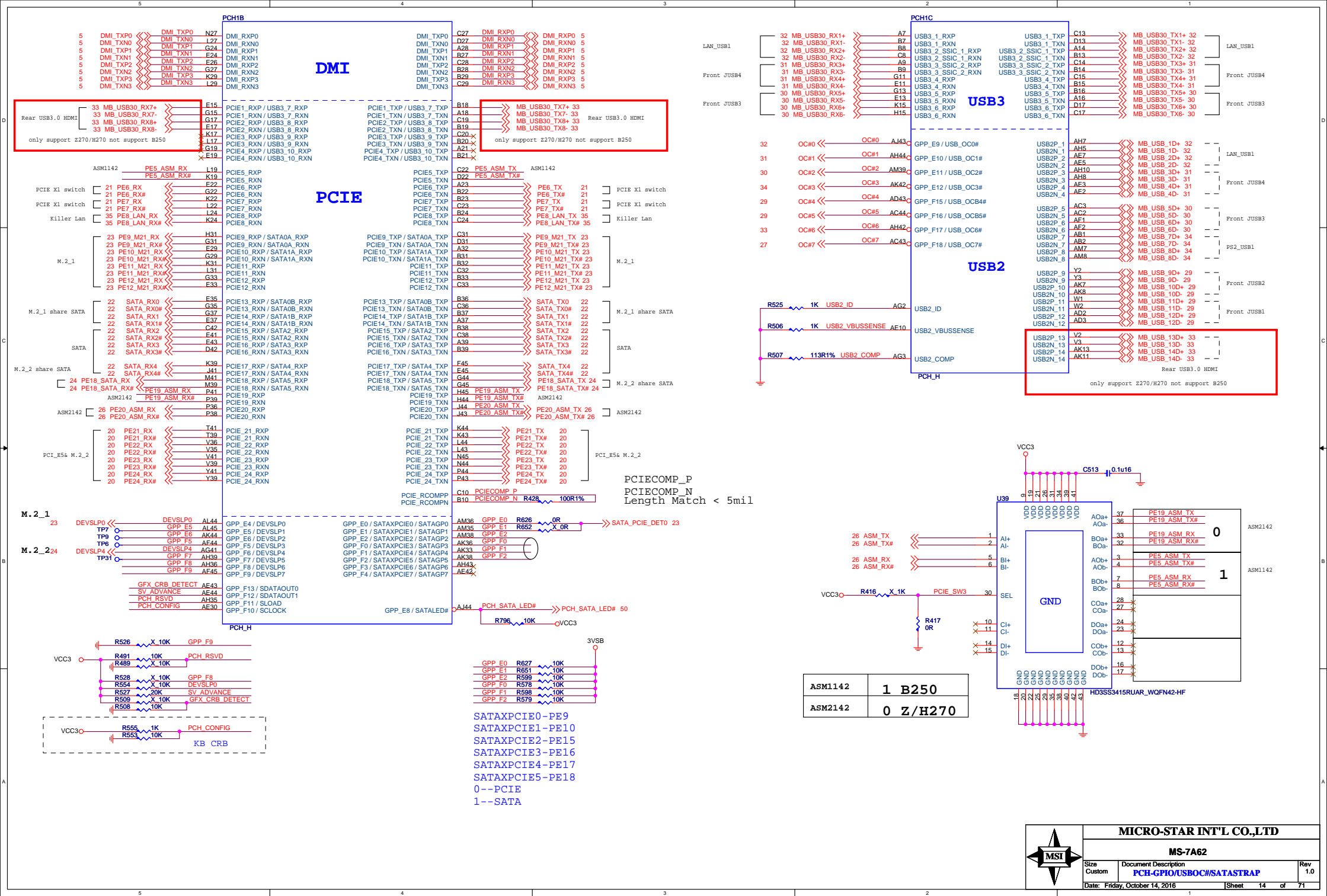


<b>MICRO-STAR INT'L CO.,LTD</b>			
<b>MS-7A62</b>			
Size Custom	Document Description <b>DDR4-POWER/GND-2</b>		Rev 1.0
Date: Friday, October 14, 2016		Sheet 11 of 71	



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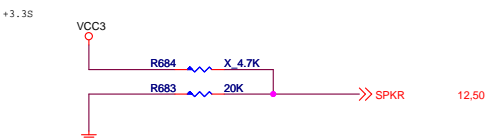




VSS

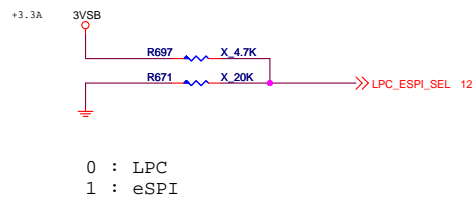


## TOP Swap



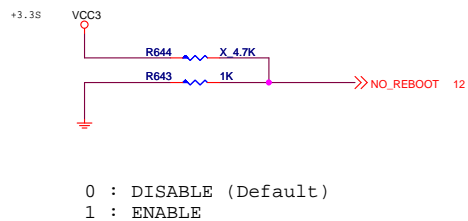
Internal pull-down is disabled after PLTRST#

## LPC eSPI Mode



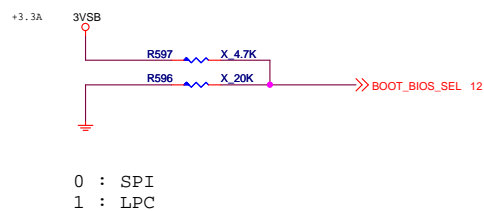
Internal pull-down is disabled after RSMRST

## No Reboot



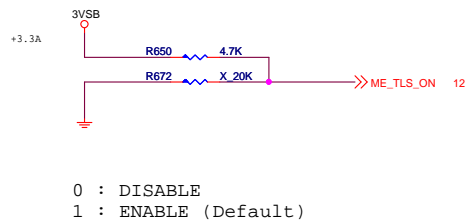
Internal pull-down is disabled after PLTRST#

## Boot BIOS



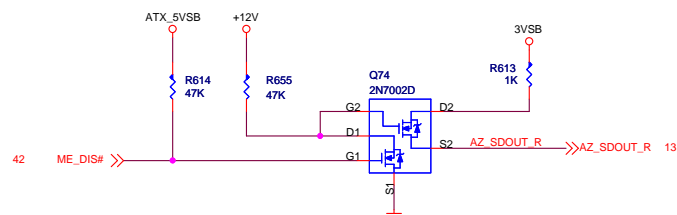
Internal pull-down is disabled after PLTRST#

## AMT and SBA with confidentiality

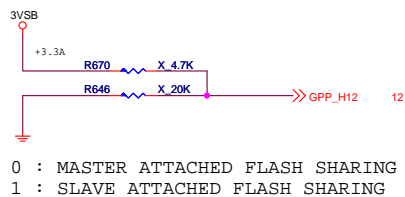


Internal pull-down is disabled after RSMRST

## HDA\_SDO



## ESPI FLASH SHARING MODE



Internal pull-down is disabled after RSMRST

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Size	Document Description	Rev
Custom	PCH-Strap	1.0
Date: Friday, October 14, 2016	Sheet 18 of 71	

Footprint: SLOT\_PCIEXP164\_13\_TEST

3VSB - 375mA



AVL:D0G-45B0510-I14

D23

4 6

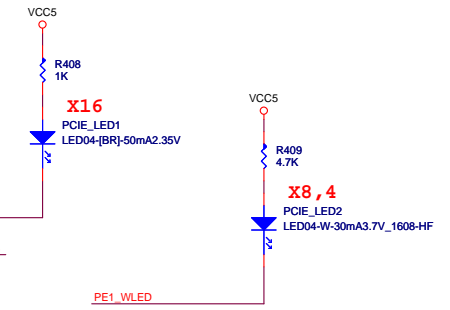
3 1

X SMBCLCK\_VSB\_R 12,20,21

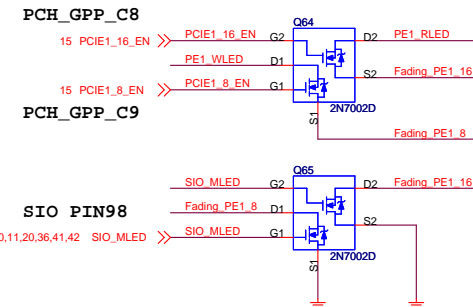
X SMBDATA\_VSB\_R 12,20,21

X\_ESD-AO28902CIL-HF

By Placement



WRT:D0C-040T200-H91  
AVL:D0C-040S200-E07



████████████████████	M.2_1
████████████████████	PCI_E1
████████████████	PCI_E2
████████████████	PCI_E3
████████████████████	PCI_E4
████████████████	PCI_E5
████████████████████	PCI_E6



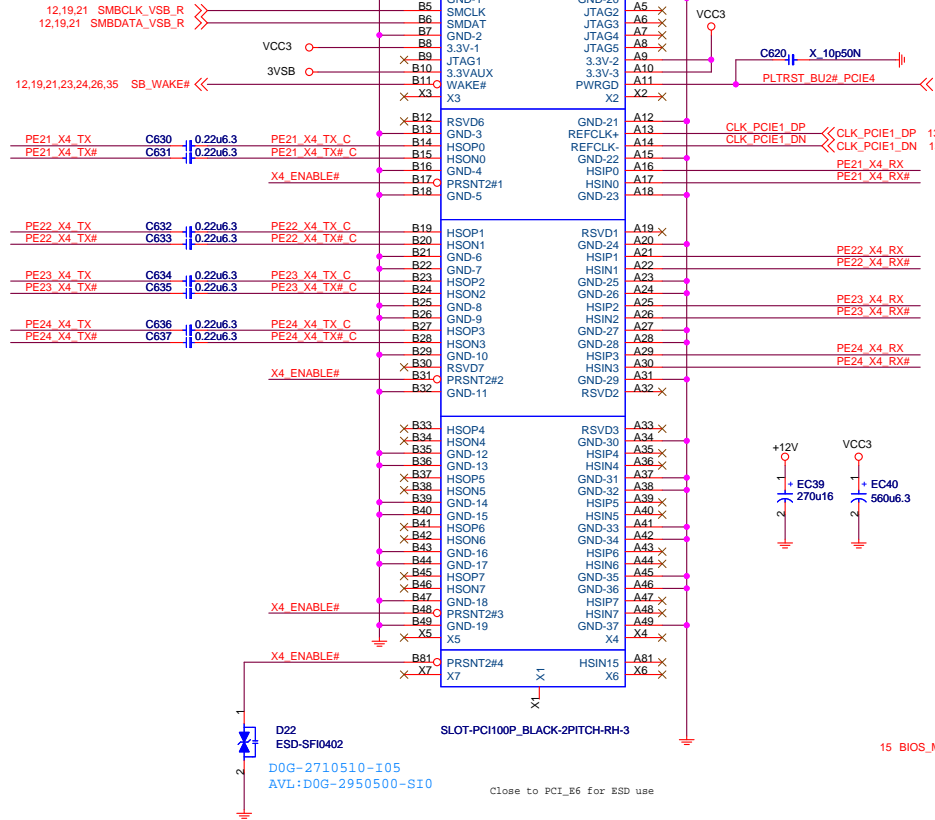
Size Custom	Document Description <b>PCIE SLOT (X16)</b>	Rev 1.0
Date: Friday, October 14, 2016	Sheet 19 of 71	

# PCI\_Express X4 slot (From PCH X4)

P/N:N11-1000221-L06  
Footprint:SLOT\_PCIEXP100\_5\_TEST

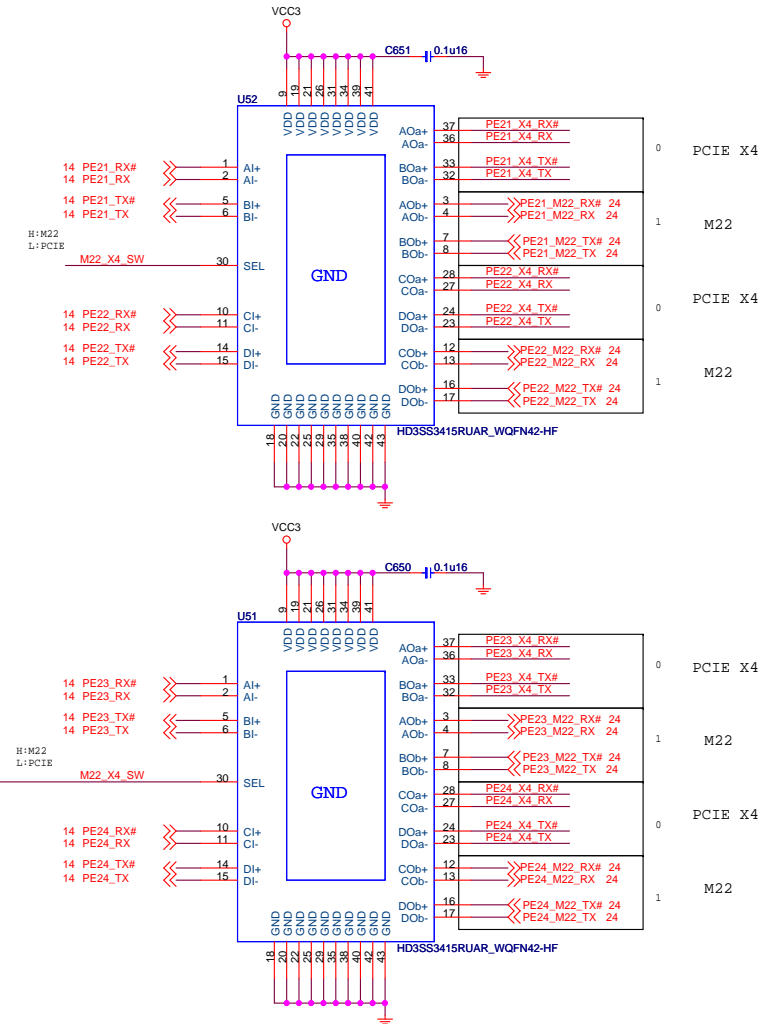
N11-1000151-L06

12V - 2.1A  
VCC3 - 3A  
3VSB- 375mA



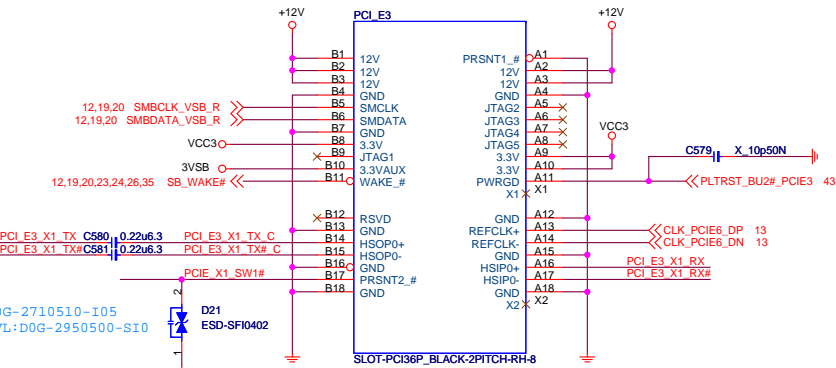
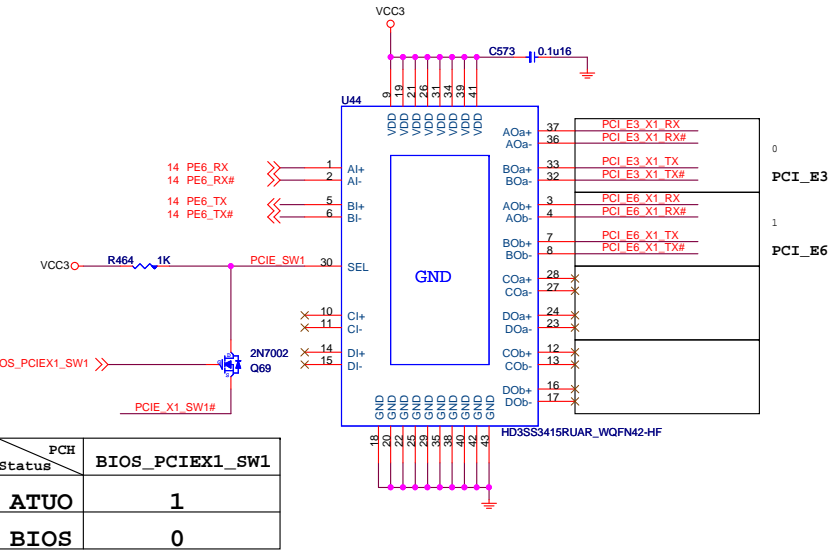
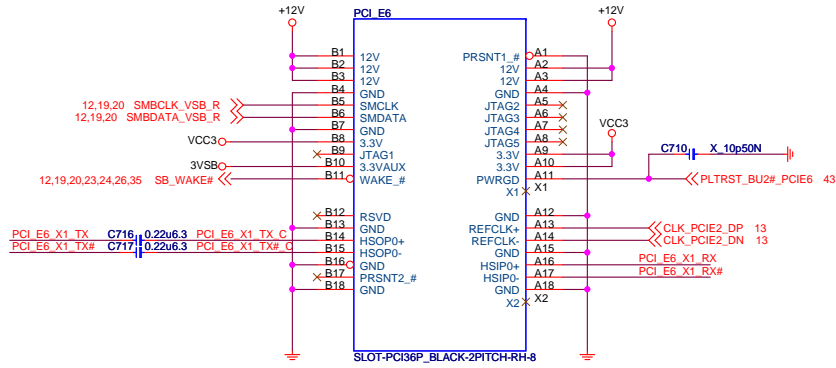
PCH Status	BIOS_M22_X4_SW
ATUO	1
BIOS	0

M22_X4_SW	
Hi	M.22
LOW	PCI_E5

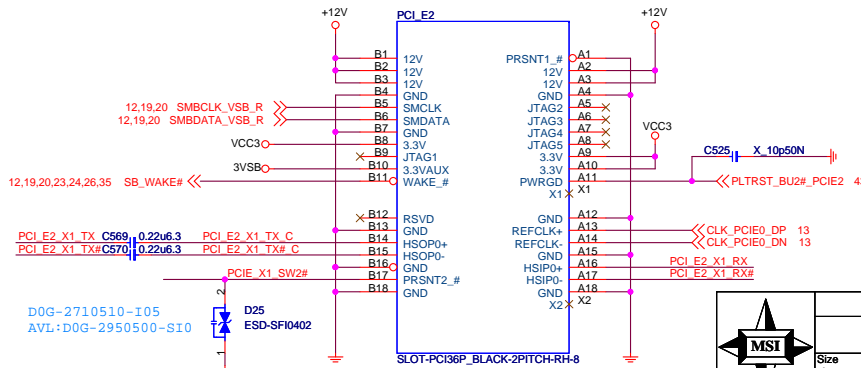
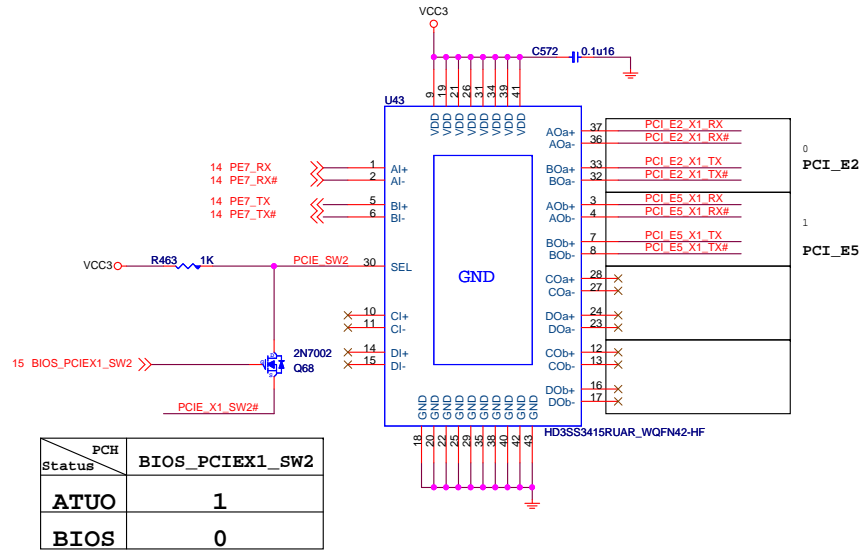
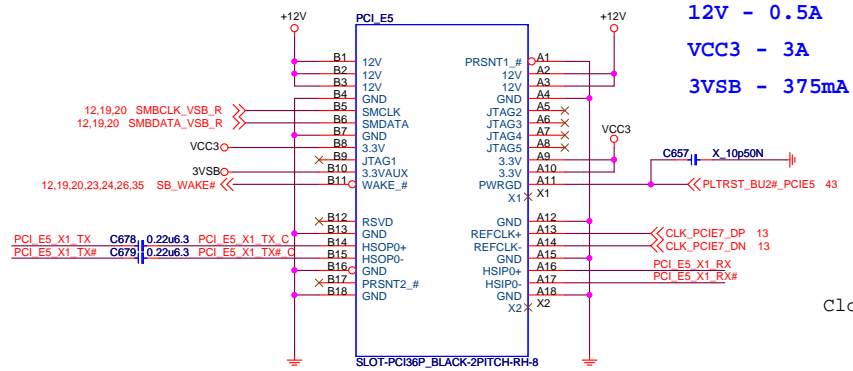


LED  
WRT:D0C-040T200-H91  
AVL:D0C-040S200-E07

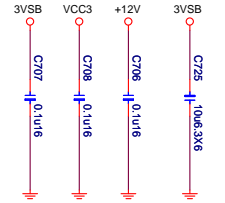
# N11-0360441-L06



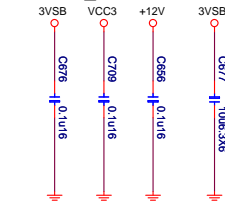
# N11-0360441-L06



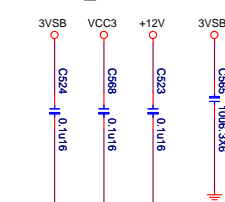
Close to PCI\_E6 for ESD use



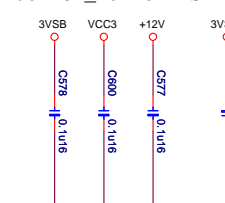
Close to PCI\_E5 for ESD use



Close to PCI\_E2 for ESD use

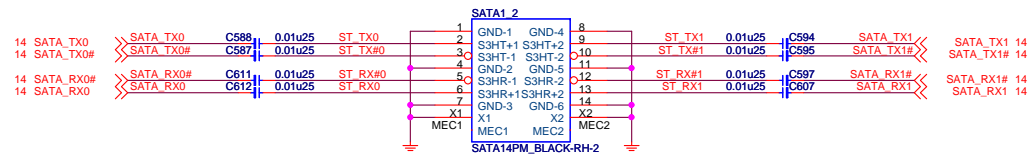


Close to PCI\_E3 for ESD use



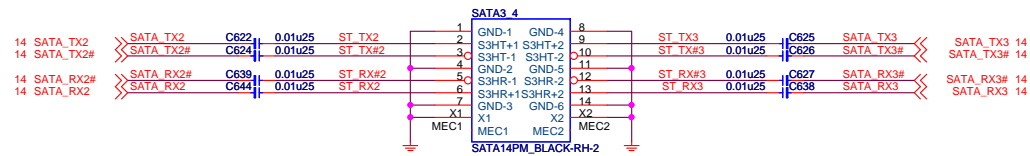
MICRO-STAR INT'L CO.,LTD		
MS-7A62		
Size	Document Description	Rev
Custom	PCIE SLOT-PCH (X1)/Switch	1.0
Date: Friday, October 14, 2016		Sheet 21 of 71

### N5N-14M0201-L06

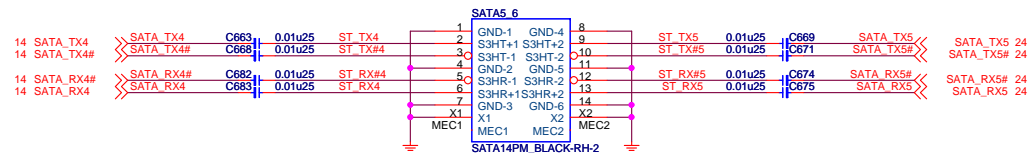


M.2\_1 use SATA Function, SATA1&SATA2 not support

### N5N-14M0201-L06



### N5N-14M0201-L06



M.2\_2 use SATA Function, SATA6 not support

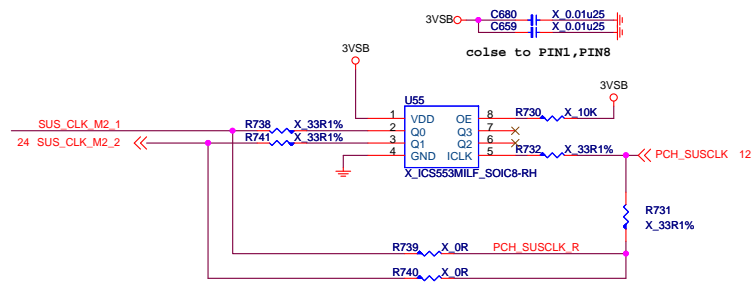


MICRO-STAR INT'L CO.,LTD

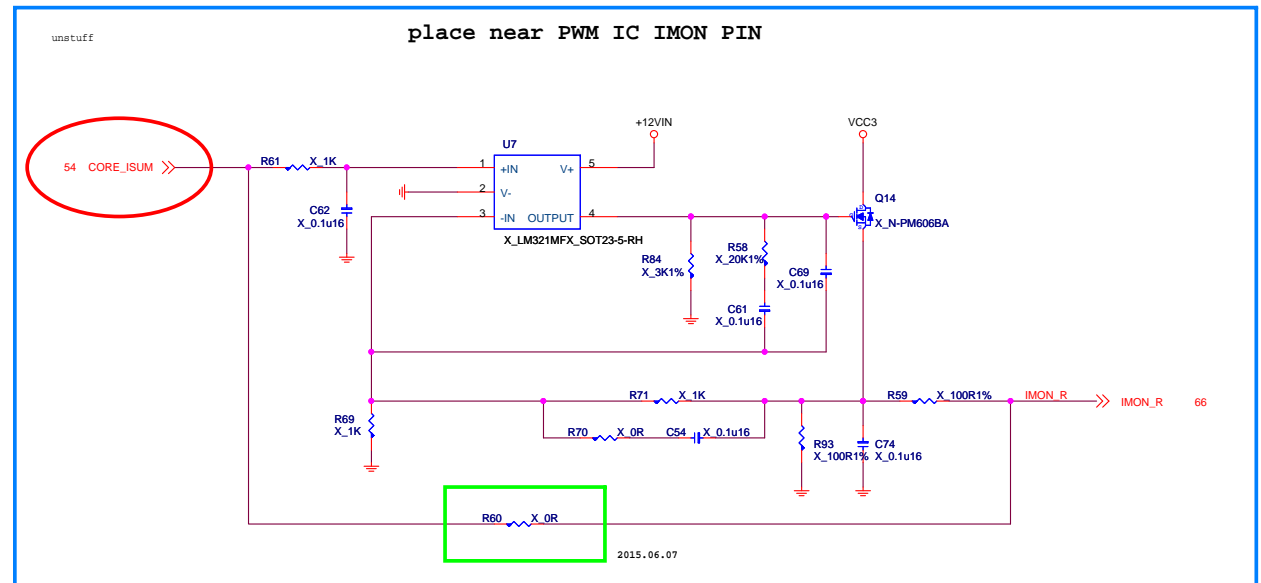
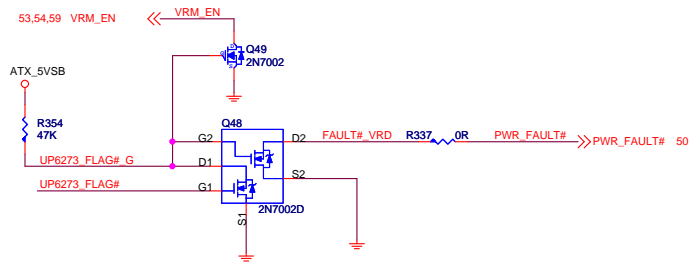
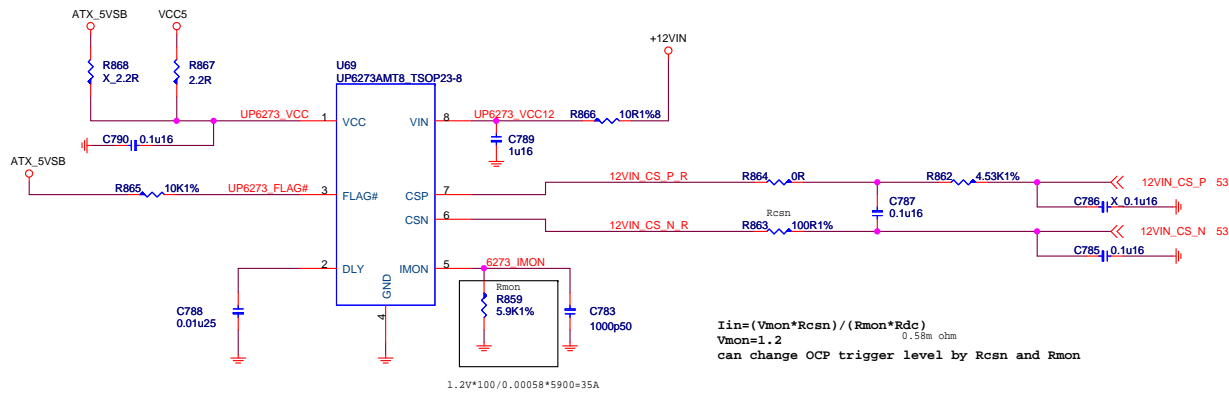
MS-7A62

Size	Document Description	Rev
Custom	SATA Connector	1.0
Date: Friday, October 14, 2016	Sheet 22 of 71	









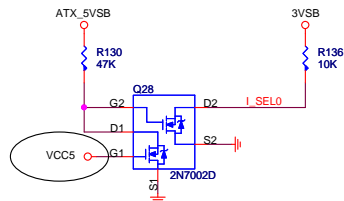
MICRO-STAR INT'L CO.,LTD

MS-7A62

Size	Document Description	Rev
Custom		1.0
Date:	Friday, October 14, 2016	Sheet 25 of 71



## Current Mode

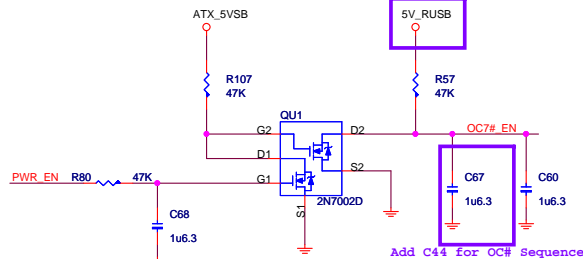


I\_SELO:I\_SEL1

X	0	Default for 900mA
0	1	1.5A @5V
1	1	3A @5V

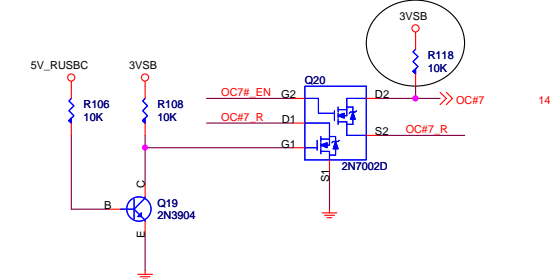
1.5A under S3 mode  
3A under S0 mode

## VBUS OC#

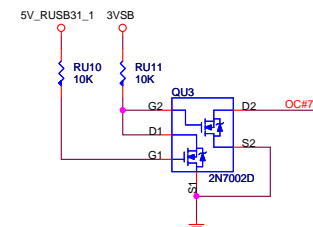
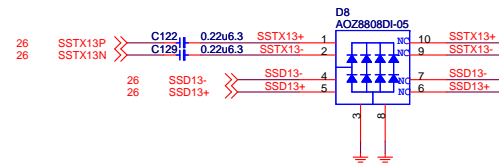


Add C44 for OC# Sequence

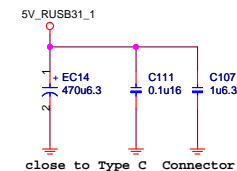
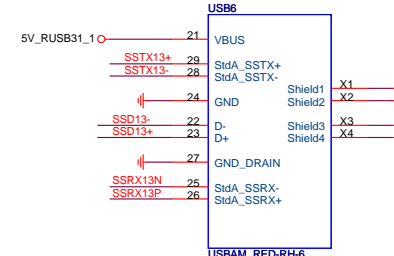
need pull hi for type c OC use



## TYPE-A

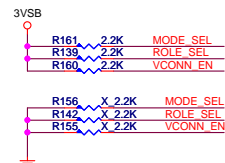


## N53-09M0861-L06



close to Type C Connector

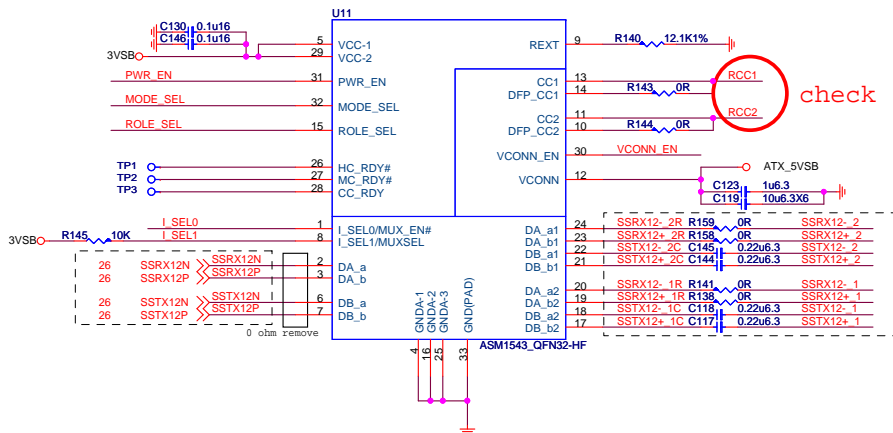
## USB Type-C MUX with Configuration Channel (CC)



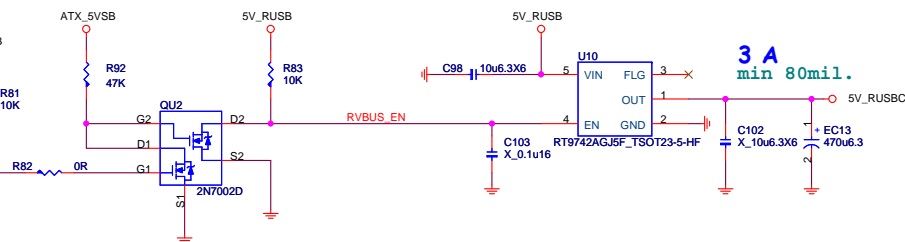
MODE_SEL	
1	CCL MODE (default)
0	Mux MODE

ROLE_SEL	
1	DFP role (default)
0	UFP role

VCONN_EN	
1	enable
0	disable



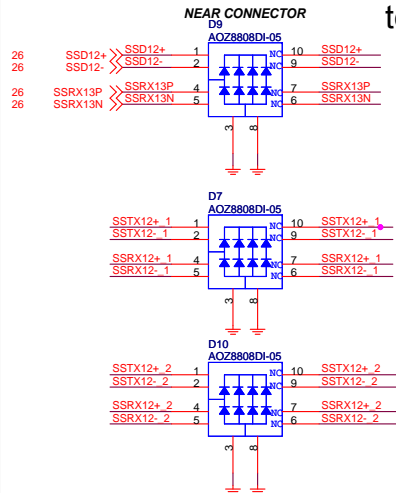
check



3 A  
min 80mil.

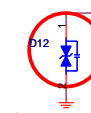
## TYPE-C

### ESD Protection



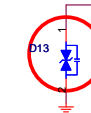
USB3.0 (ESD)  
D0G-06A030C-A68 (M)  
D0G-05A0300-I14  
D0G-06A050C-A68  
D0G-05A056C-I05  
D0G-45B031C-005

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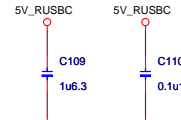
ESD-AOZ8131DI-06-HF

USB3.0 (ESD)  
D0G-12A060C-A68 T-type 分支需小於140mils

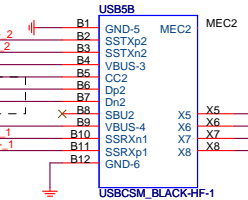
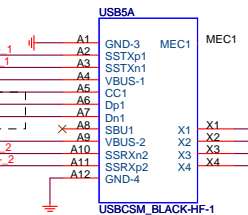


ESD-AOZ8131DI-06-HF

close to Type C Connector



## N53-24M0180-L06



MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	USB TYPE C	1.0
Date: Friday, October 14, 2016	Sheet 27 of 71	

VCC5V

ATX\_PWR\_OK

5VUSB5V

5VSDRV2

5VCC\_DRV

5VDRV2

12V

uP7501

MODE

USB\_MODE

SLP\_S3#

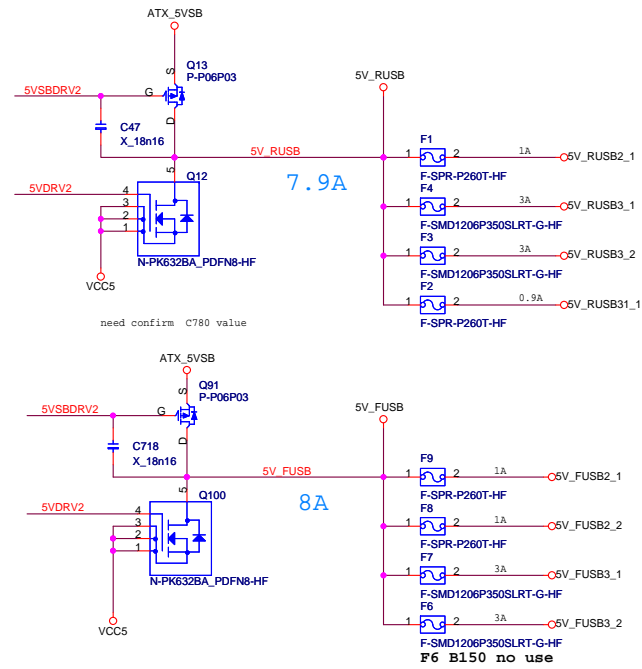
SLP\_S4#

H: SUPPORT S0/S3/S5

L: SUPPORT S0/S3

need keep ,when using sIO control

5VDRV2, 5VSDRV2 width 12mil,  
Do NOT route near the edge of a



3.5A(Itrip=3.5A; 0.003ohm)  
D08-2000400-P16  
D08-2000400-L07  
2.6A (Itrip=2.6A; 0.015ohm)  
D08-0301000-P16  
D08-0301100-B07

D08-2000400-P16

2.6A (Itrip=2.6A; 0.015ohm)

D08-0301100-B07

P-MOS  
D03-06P0319-N03

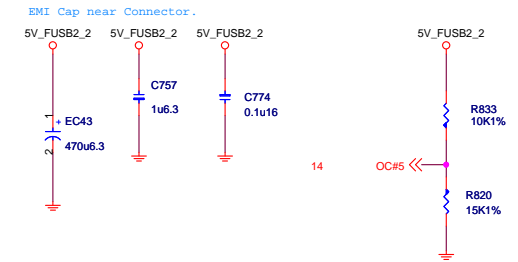
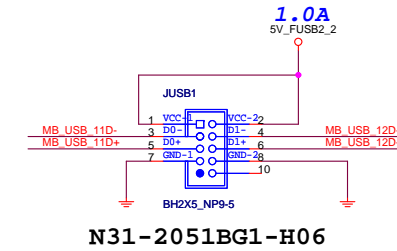
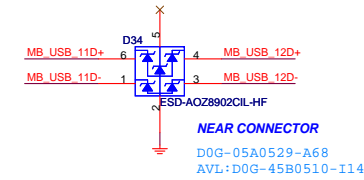
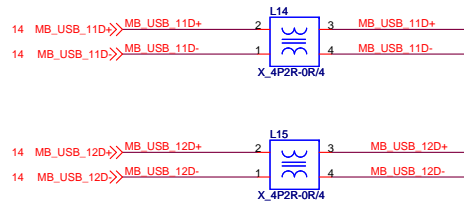
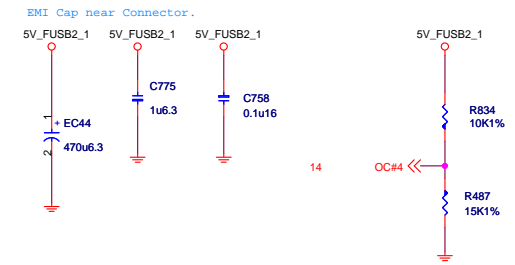
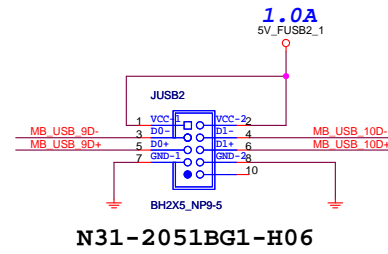
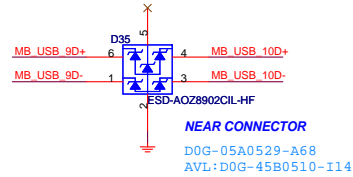
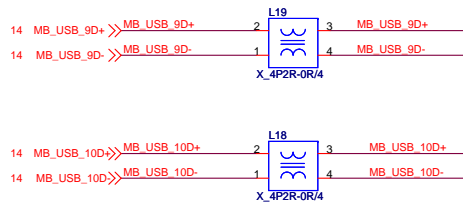
N-MOS  
D03-510BA0C-N03

D03-3830D09-N47

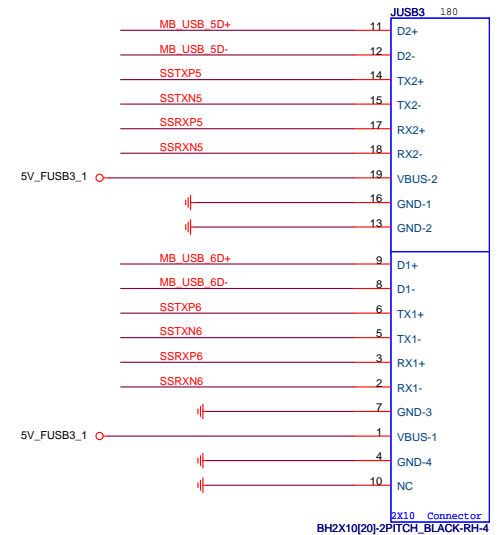
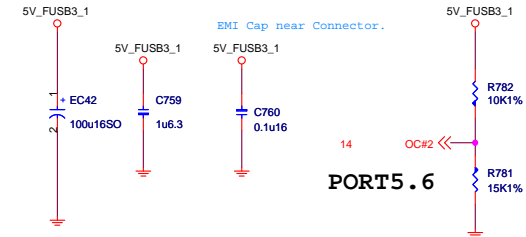
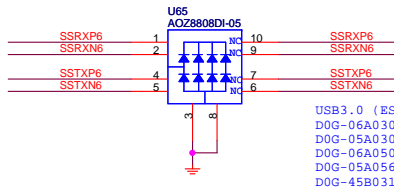
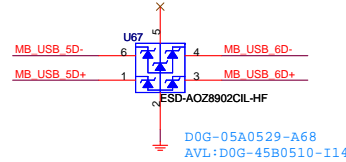
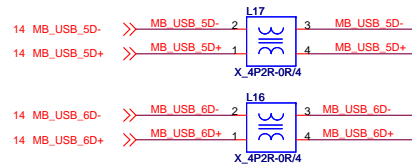
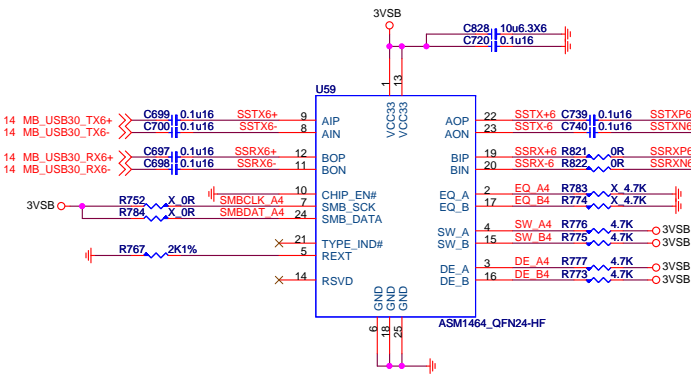
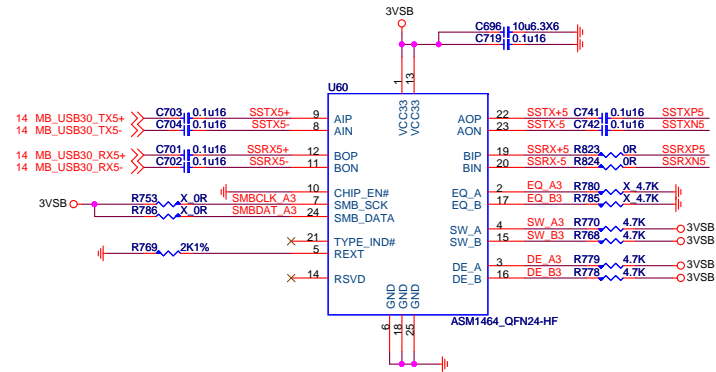


MS-7A62

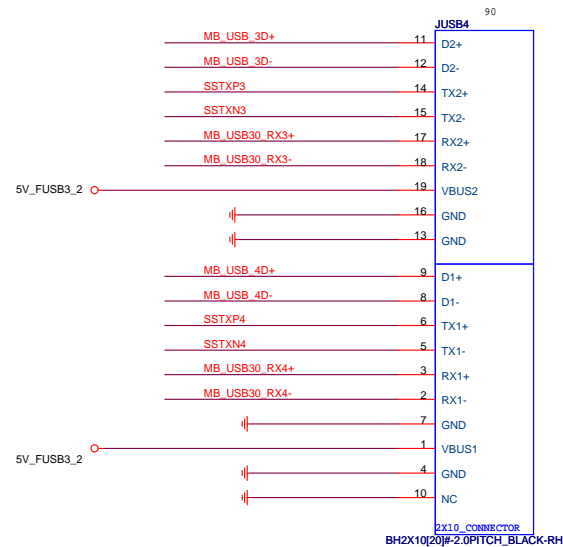
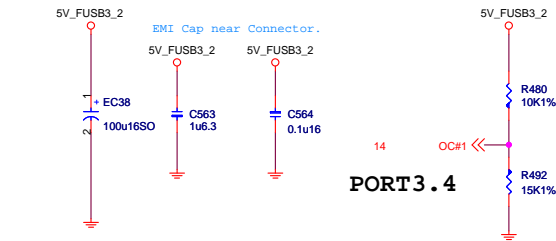
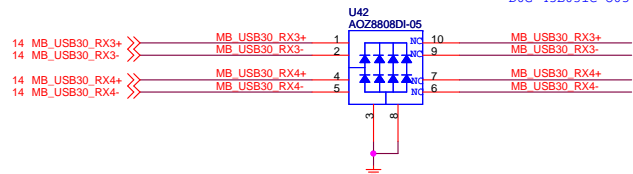
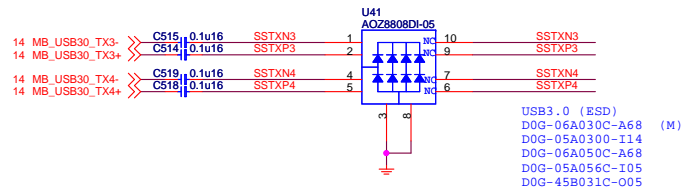
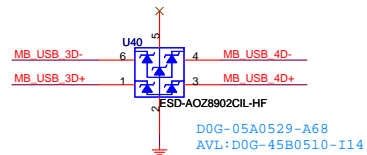
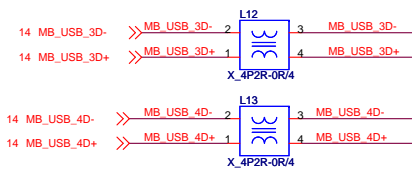
Size Custom	Document Description <b>USB POWER UP7501</b>	Rev 1.0
Date: Friday, October 14, 2016		Sheet 28 of 71







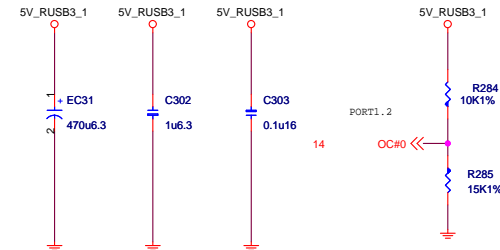
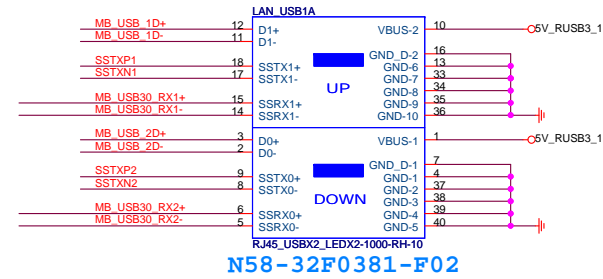
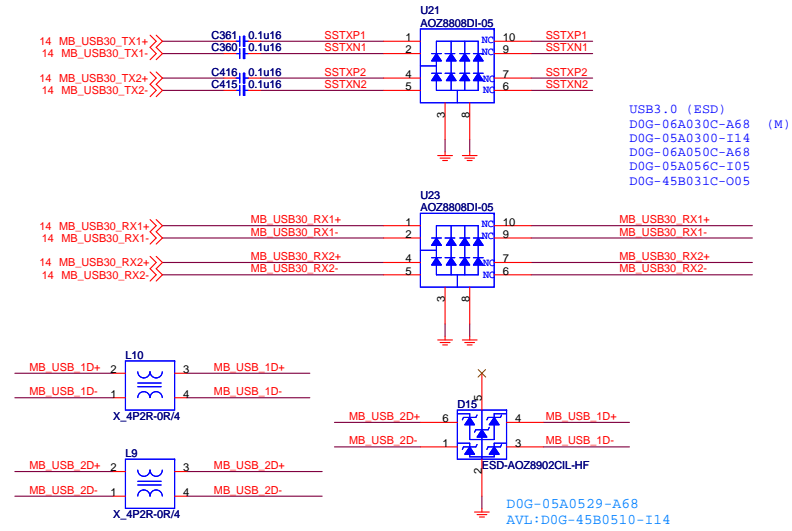
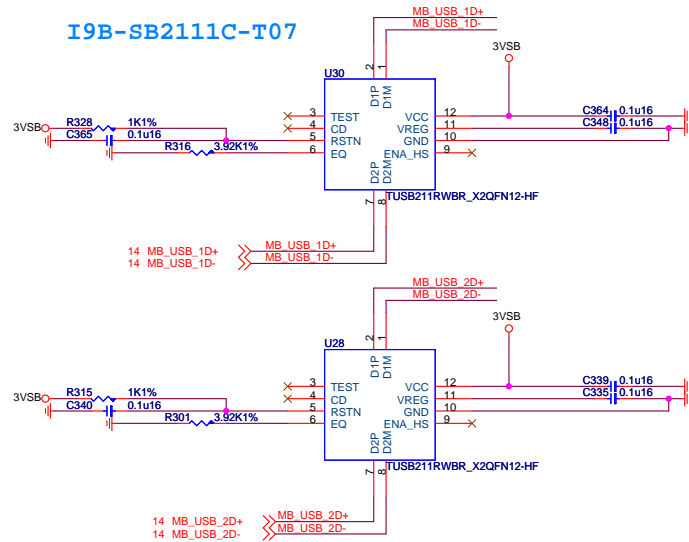
**N32-2101221-H06**

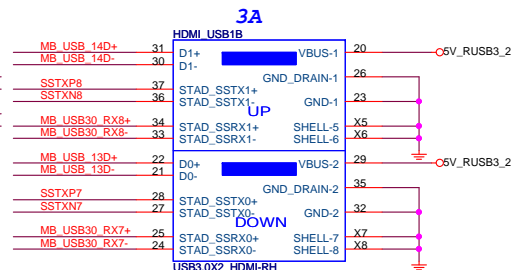
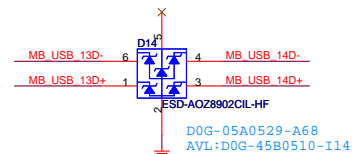
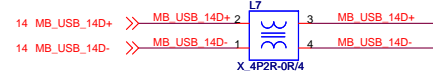
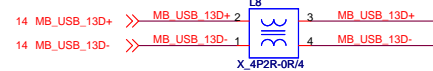
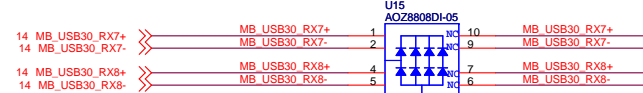
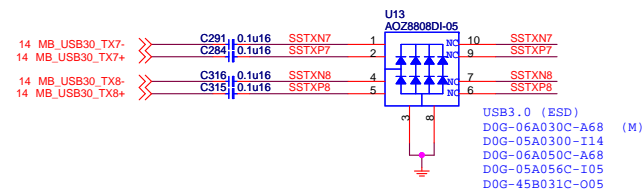
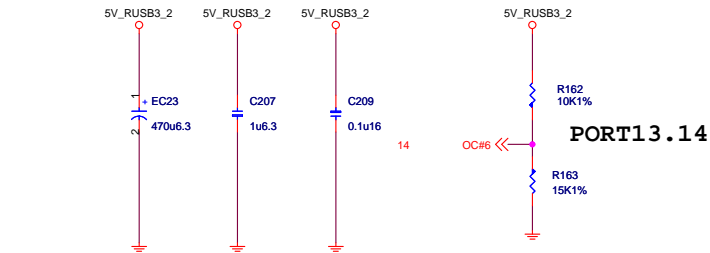


N32-2101131-H06

# LAN USB3.0 VR PORT H270/B250 no VR function remove redriver u3.

I9B-SB2111C-T07

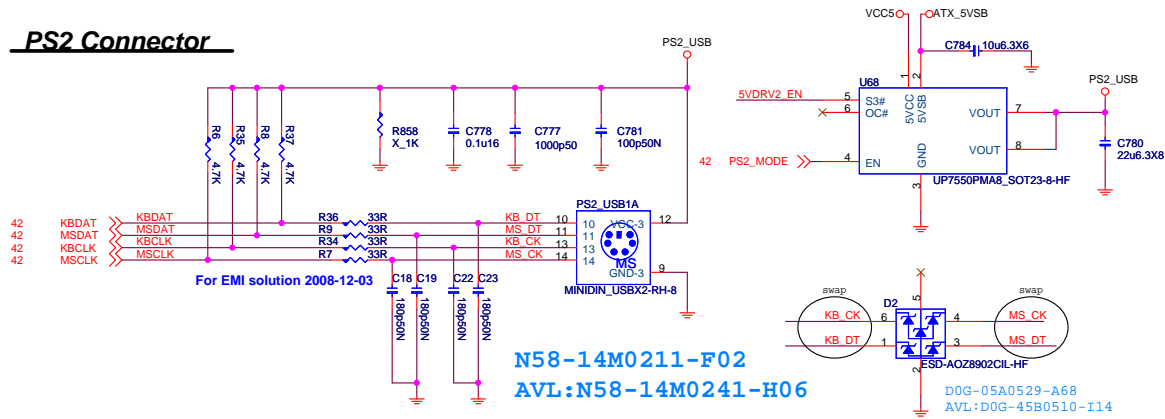




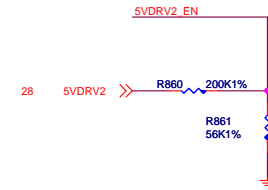
only support Z270/H270  
not support B250  
remove redriver u3.u2

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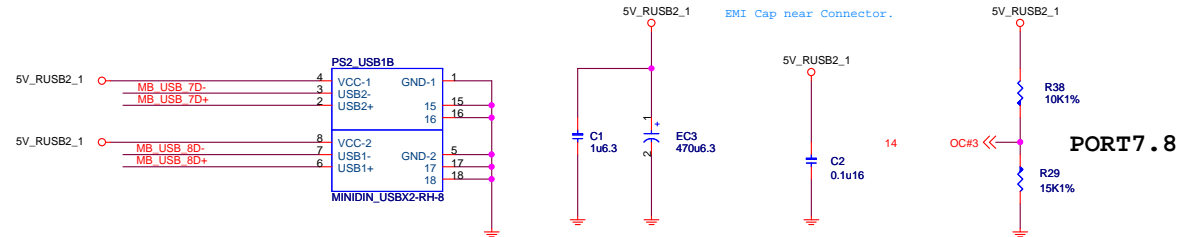
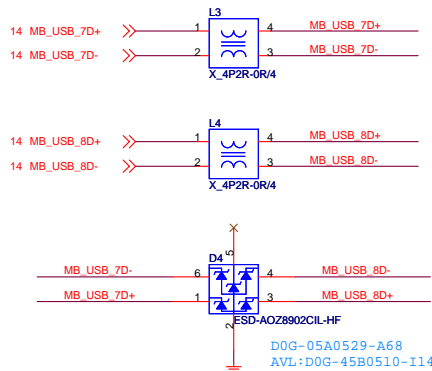
## PS2 Connector



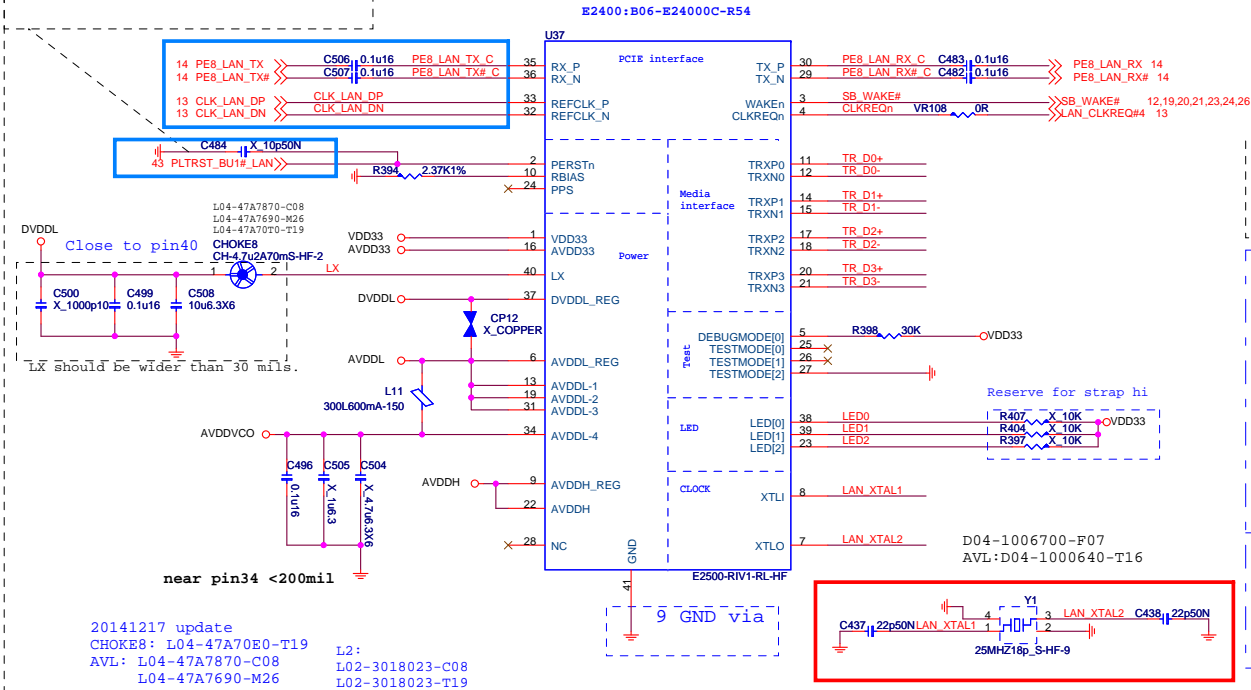
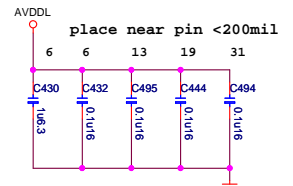
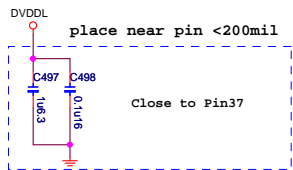
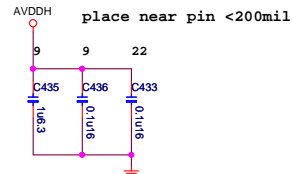
## 0.5A USB MODE



## PS\_USB1 Connector



B06-E25000C-R54 colay B06-E24000C-R54



```
VDD33 >= 30mils;  
AVDD33 >= 30mils;  
AVDDH >= 20mils;  
AVDDL >= 20mils.  
DVDDL >= 20mils.  
Pin LX to L1 >= 3
```

Close to LAN conn.

LED0\_ACT LED1\_LINK1000# LED2\_LINK100#

CL2 CL3 CL4

470p50 470p50 470p50

USB3.0 (ESD)

DOG-06A030C-A68 (M)

DOG-05A0300-I14

DOG-06A050C-A68

DOG-05A056C-I05

DOG-45B031C-005

20151109 update

C295

9in10

TCT

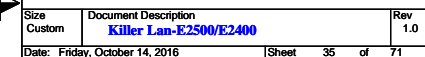
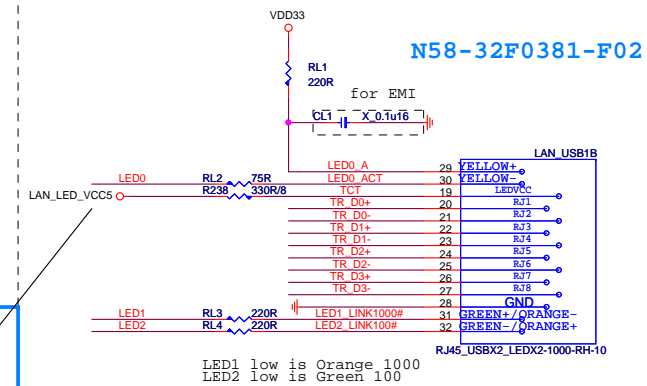
DL1

ESD-VPORT0603L102KV05-HF

Main:DOG-1020530-I05

AVL :DOG-8010510-SIO

Close to LAN conn.

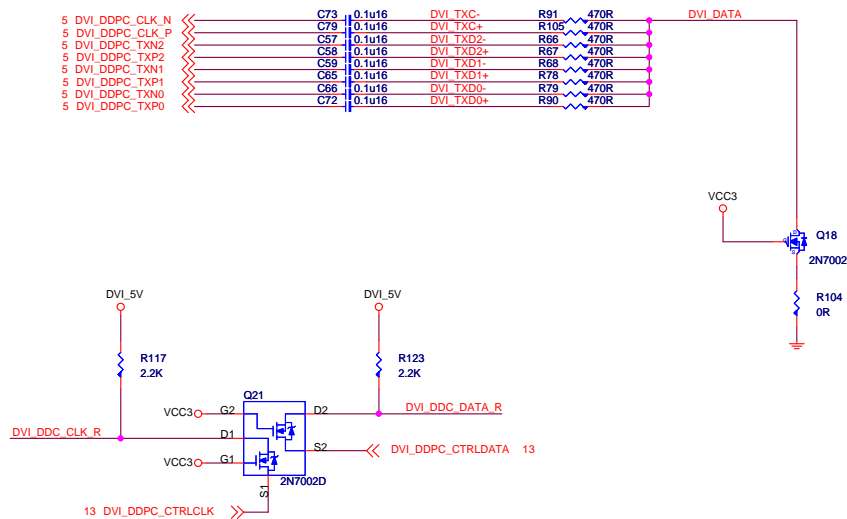


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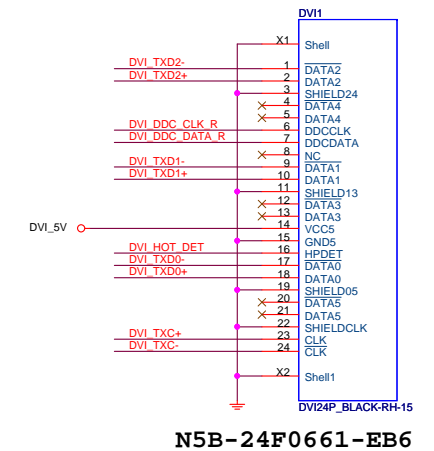
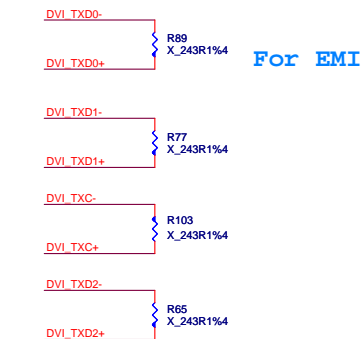
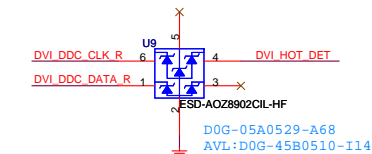
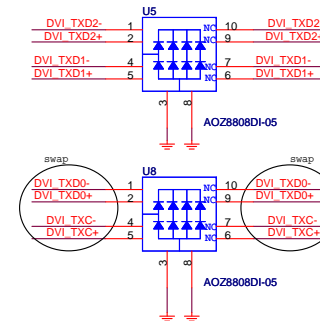
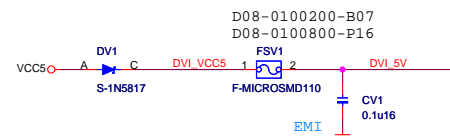
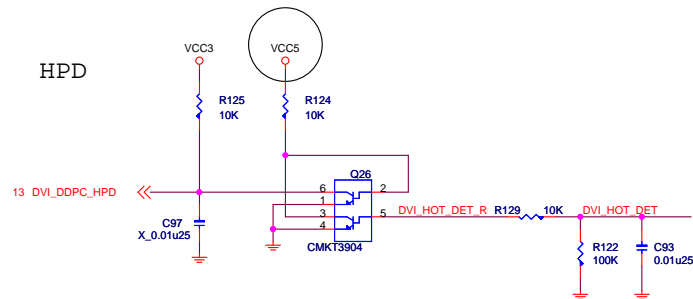


# DVI level shifter

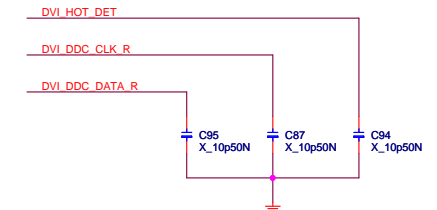
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



HPD



N5B-24F0661-EB6

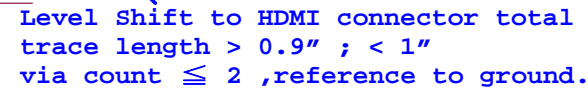


MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	DVI	1.0
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MAX Trace Length 5.5"  
reference to ground.



NXP :9.09K  
ASMEDIA:3K

note

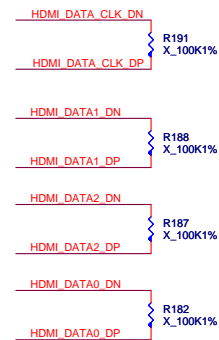
internal pull-up at  
~500K ohm.  
internal pull-down at ~500K ohm.

internal pull-down at ~500K ohm.

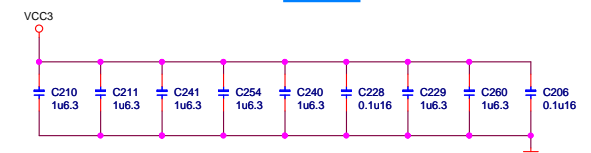
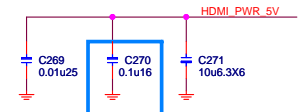
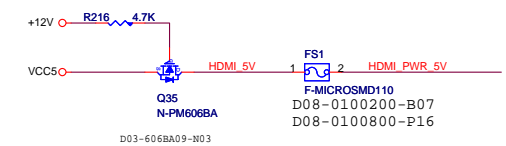
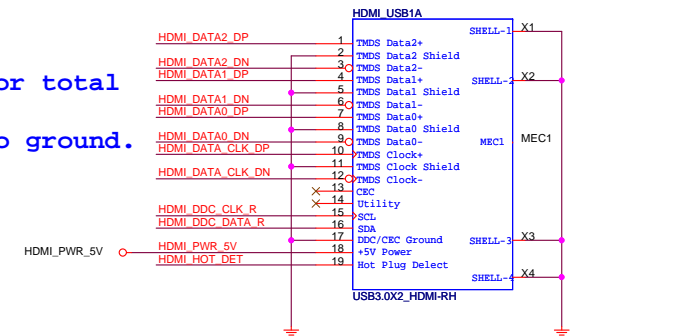
internal pull-down at ~200K ohm;  
5V tolerant.


analog current generation.

EMI



Port	Digital Display Interface Differential Pairs	HDMI Signals	PCH Digital Display Interface Pins
Port B	DDSP_B_TX0_ON	TMDSB_DATA2#	DDPB_ON
	DDSP_B_TX0_DP	TMDSB_DATA2	DDPB_OP
	DDSP_B_TX1_ON	TMDSB_DATA1#	DDPB_1N
	DDSP_B_TX1_DP	TMDSB_DATA1	DDPB_1P
	DDSP_B_TX2_ON	TMDSB_DATA0#	DDPB_2N
	DDSP_B_TX2_DP	TMDSB_DATA0	DDPB_2P
	DDSP_B_TX3_ON	TMDSB_CLK#	DDPB_3N
	DDSP_B_TX3_DP	TMDSB_CLK	DDPB_3P
	DDPB_HPD	DDSP_B_HPD0	Hot plug detect used by HDMI Port B.
	SDVO_CTRLCLK	HDMIb_CTRL_CLK	HDMI DDC lines for Port B
SDVO_CTRLDATA	HDMIb_CTRL_DATA		



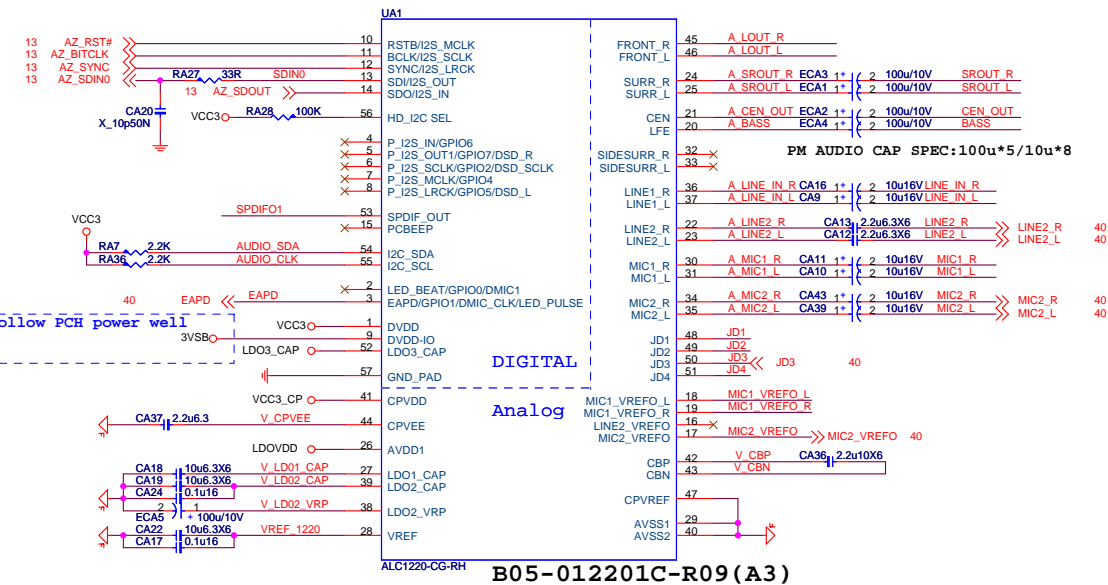
	<b>MICRO-STAR INT'L CO.,LTD</b>			
	<b>MS-7A62</b>			
	Size Custom	Document Description <b>HDMI Connector</b>		Rev 1.0
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	"0"	"1"
DDC_EN	DDC level shifter disable	DDC level shifter enable
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances
OE#	enable	the chip is power down and input termination resistors will be at high impedance.
HPD_SINK	disable	enable
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.	
REXT		

[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

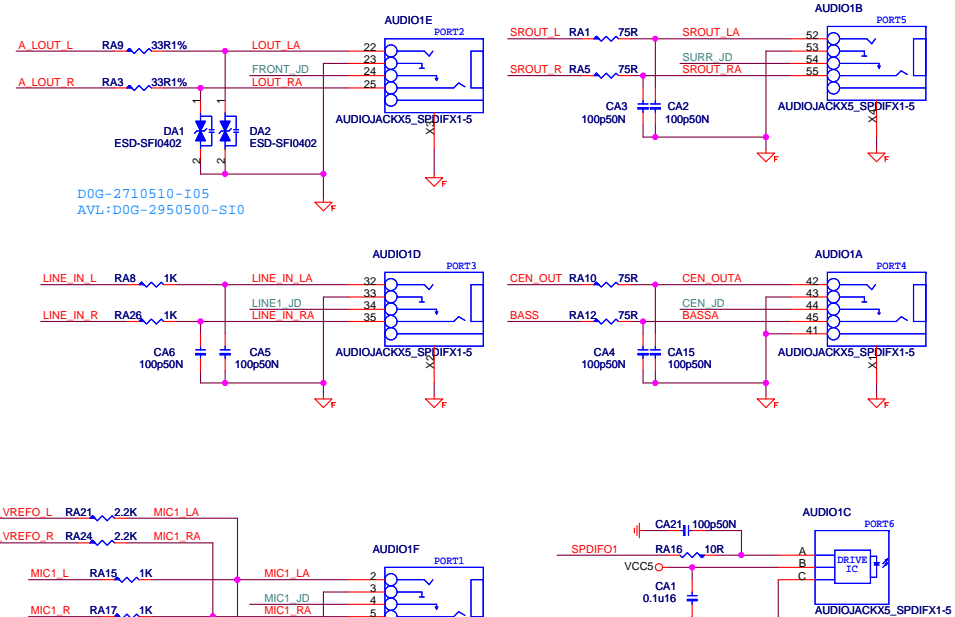
PULL-DOWN		note
PC1, PC0		
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	

# ALC1220

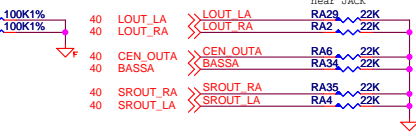
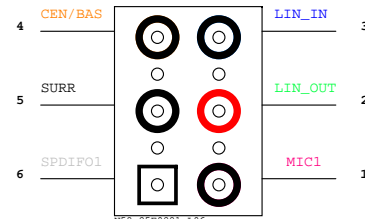


follow PCH power well

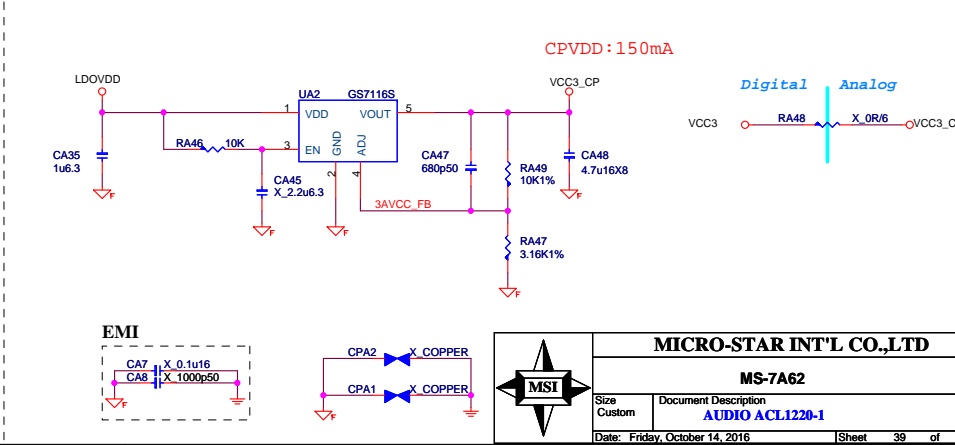
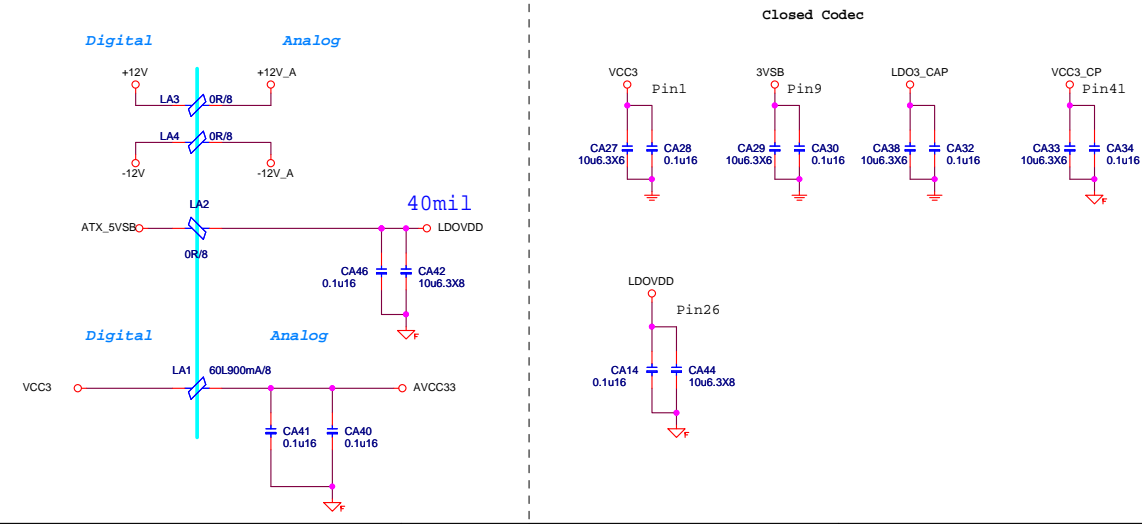
all of JD resistors should be placed as close as possible to the sense pin of codec.



## N58-25F0271-L06



CPVDD POWER: ATX5VSB will Leakage to CVDD by ALC1220, so CVDD must keep 3.3V

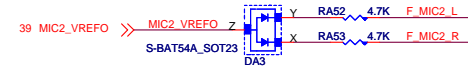
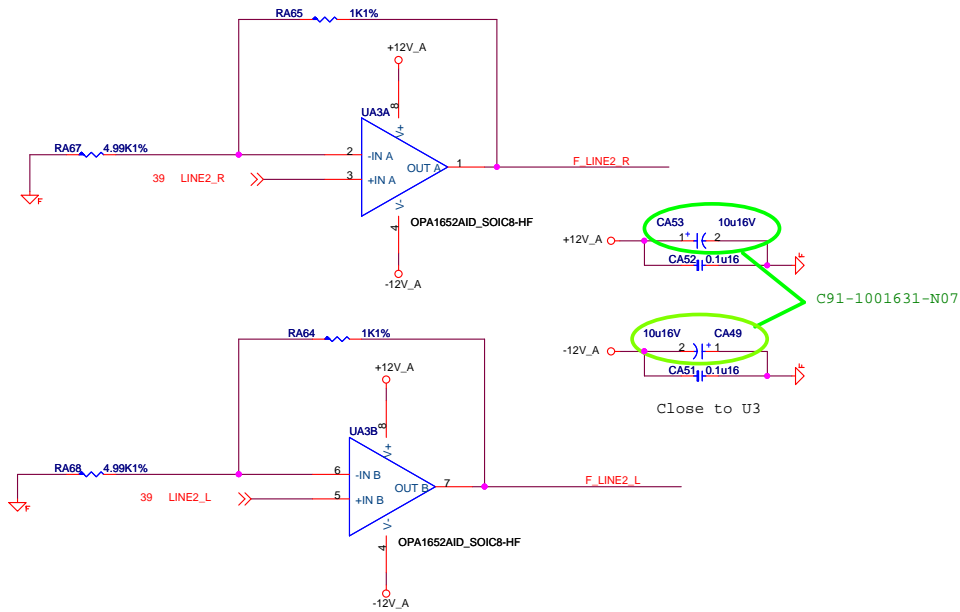


**MICRO-STAR INT'L CO.,LTD**

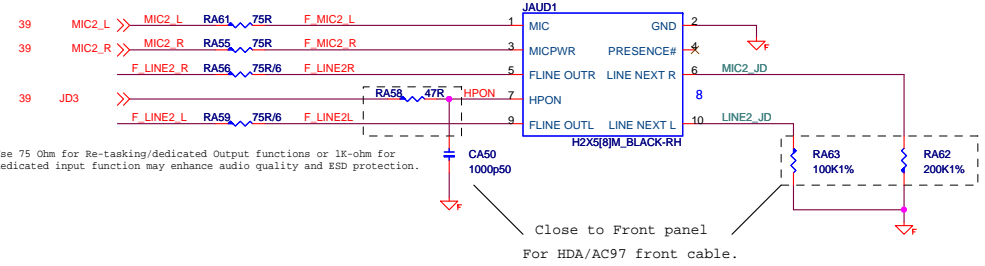
**MS-7A62**

Size Custom Document Description **AUDIO ACL1220-1** Rev 1.0

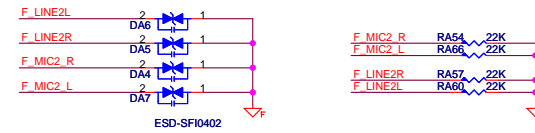
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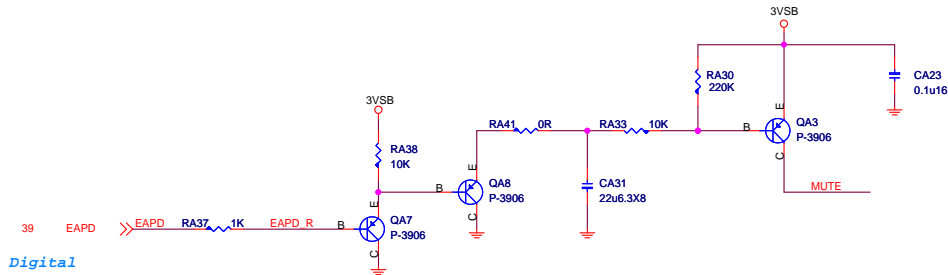
N31-2051411-H06



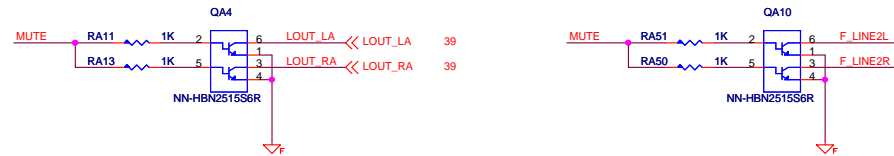
**ESD protect**  
Close to Jack  
D0G-2710510-I05  
AVL:D0G-2950500-SI0



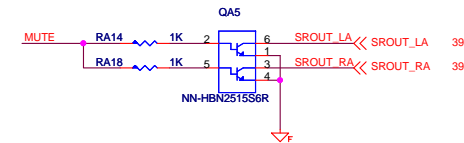
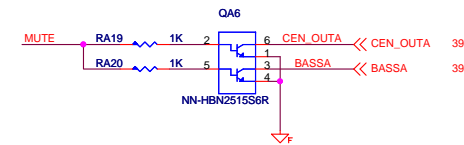
### Rear Line OUT De-POP circuit (De-pop circuit for Rear Line out & Front Headphone out)



Analog

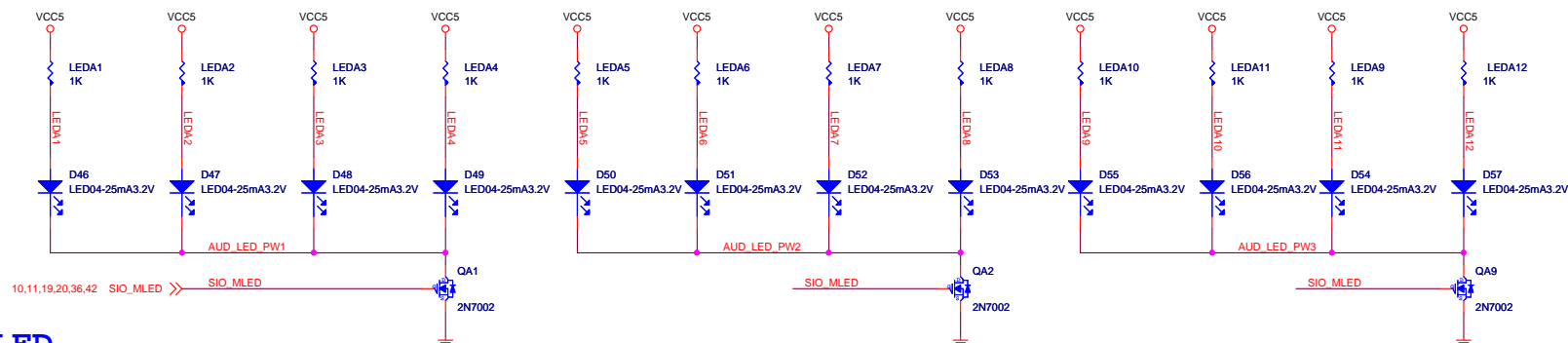


(add de-pop circuit by PM spec or customer request,  
NOTE: add de-pop circuit need to change CA6, CA7, CA12, CA13, CA23, CA24 to TVS)



0.16w\*12=1.92w  
1.92w/5=0.384A

Audio moat is transparent and width 40mil



LED

RED:D0C-040S600-E07

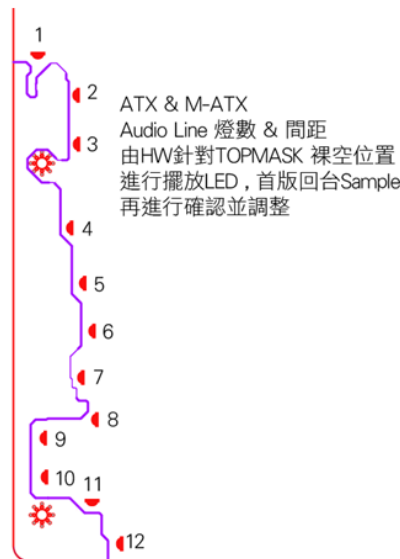
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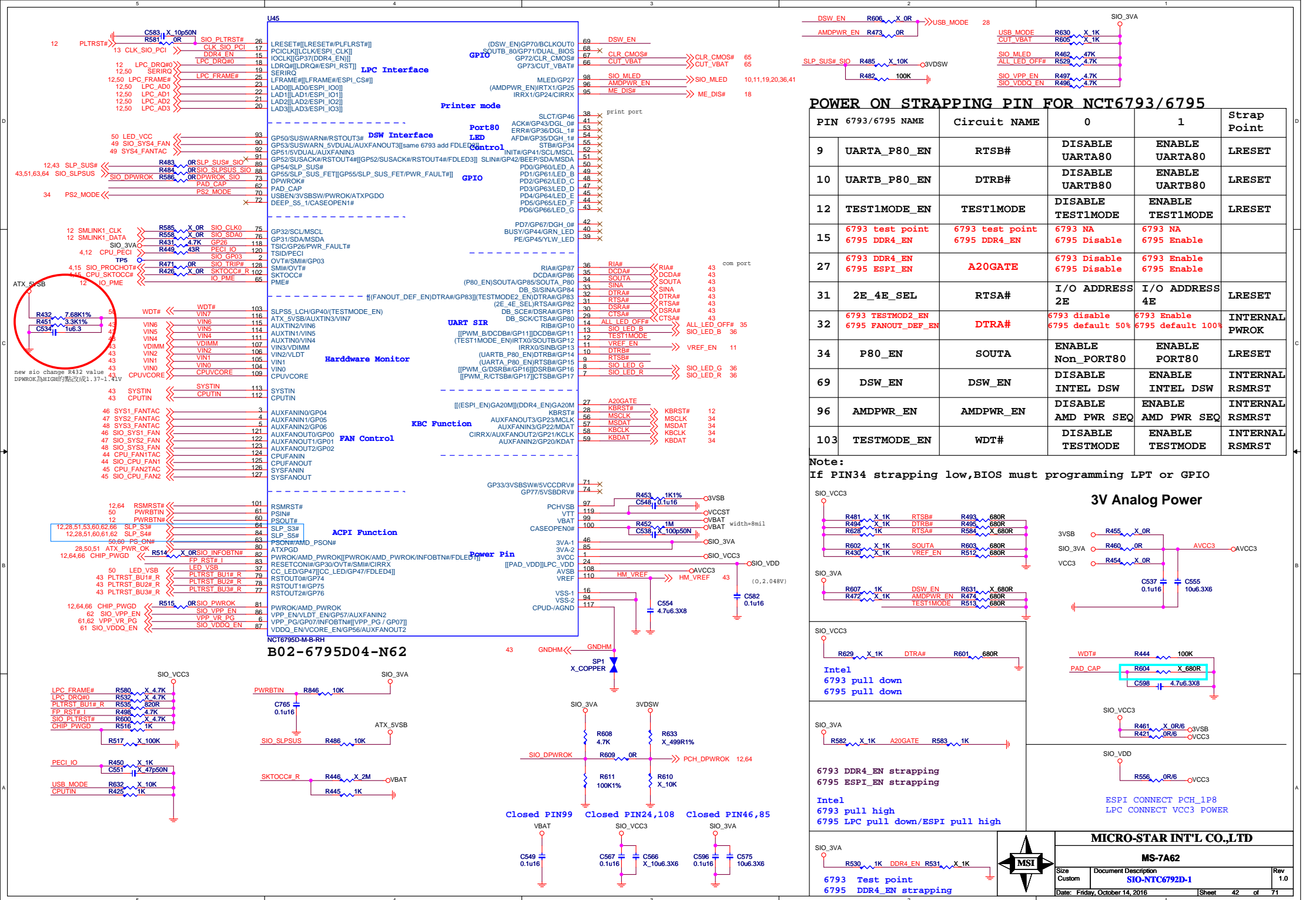
置於HS 背後需與國格  
討論，LED總功率算法  
：每顆燈0.16W X  
(Final 總燈數)

E21-7978010-A91  
20\*19.15\*8.6mm

E21-7980010-A91  
14\*12.2\*6.6mm

By Model

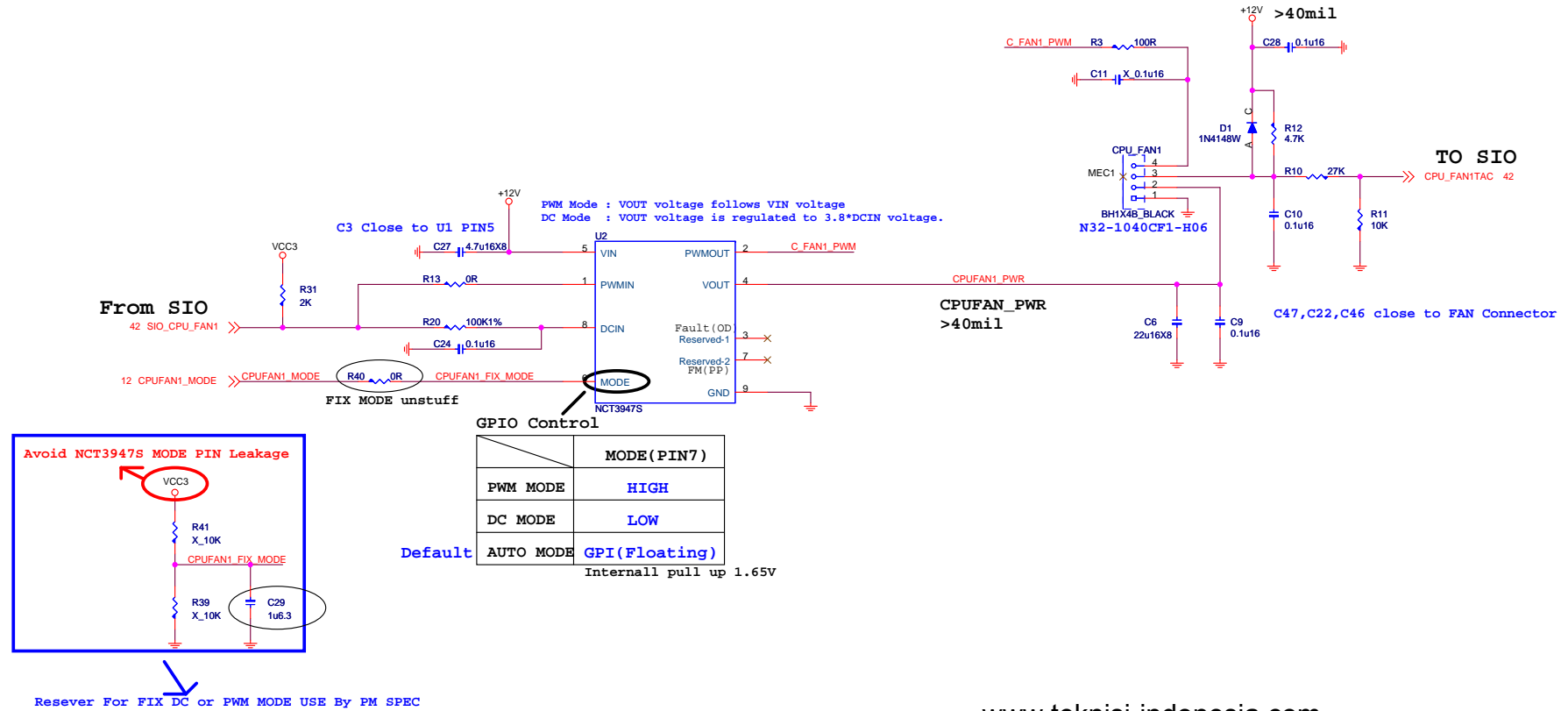






# TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

## 2.GPIO可以由BIOS切换 PWM/DC MODE

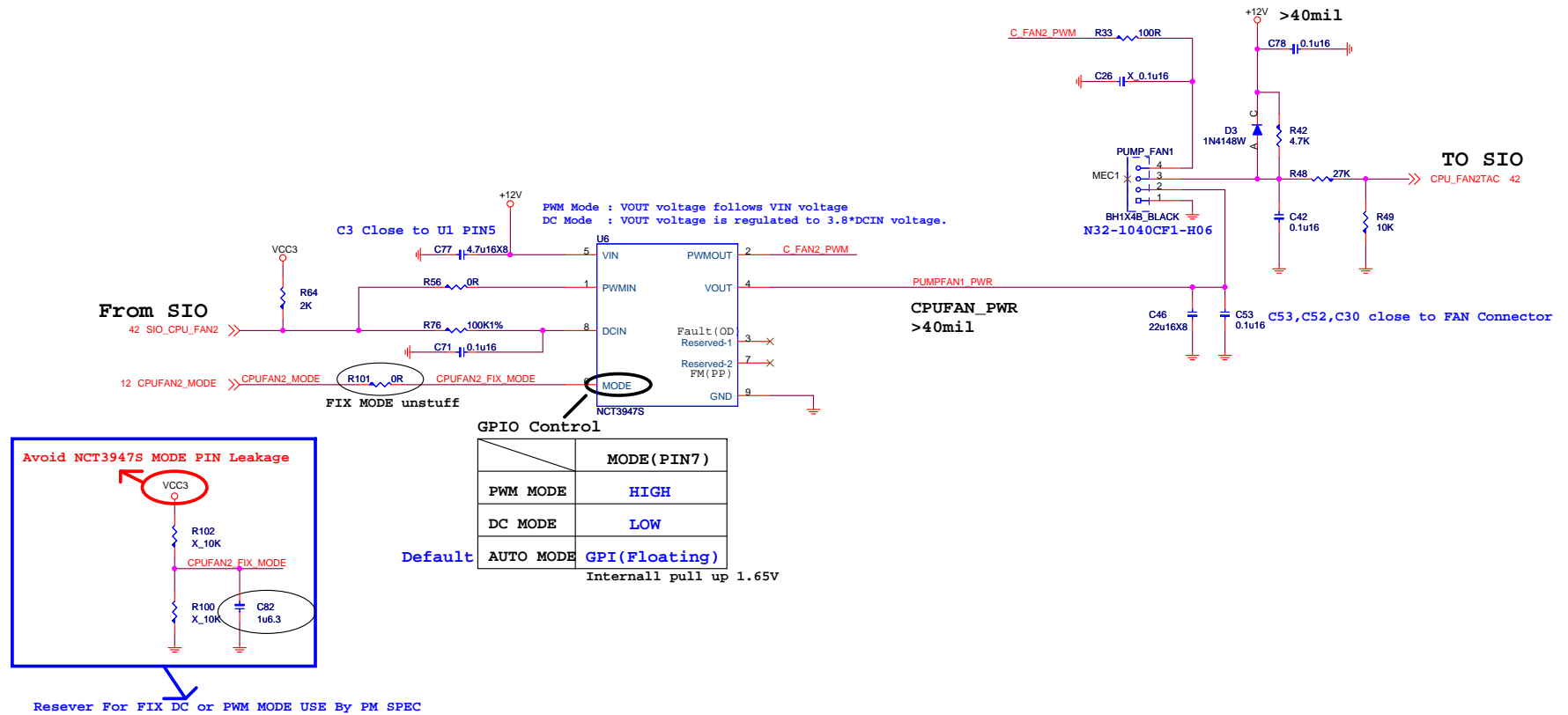


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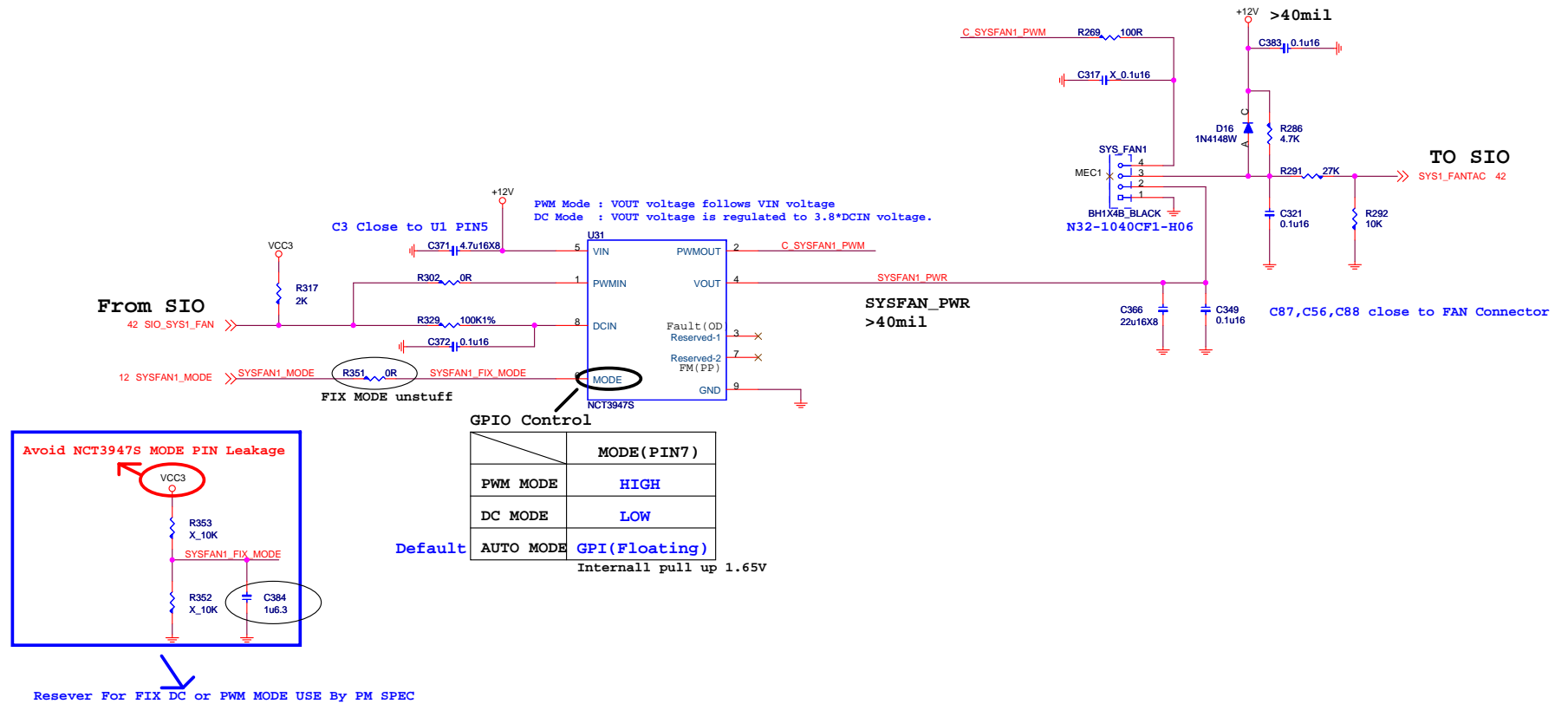
# TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

## 2.GPIO可以由BIOS切换 PWM/DC MODE



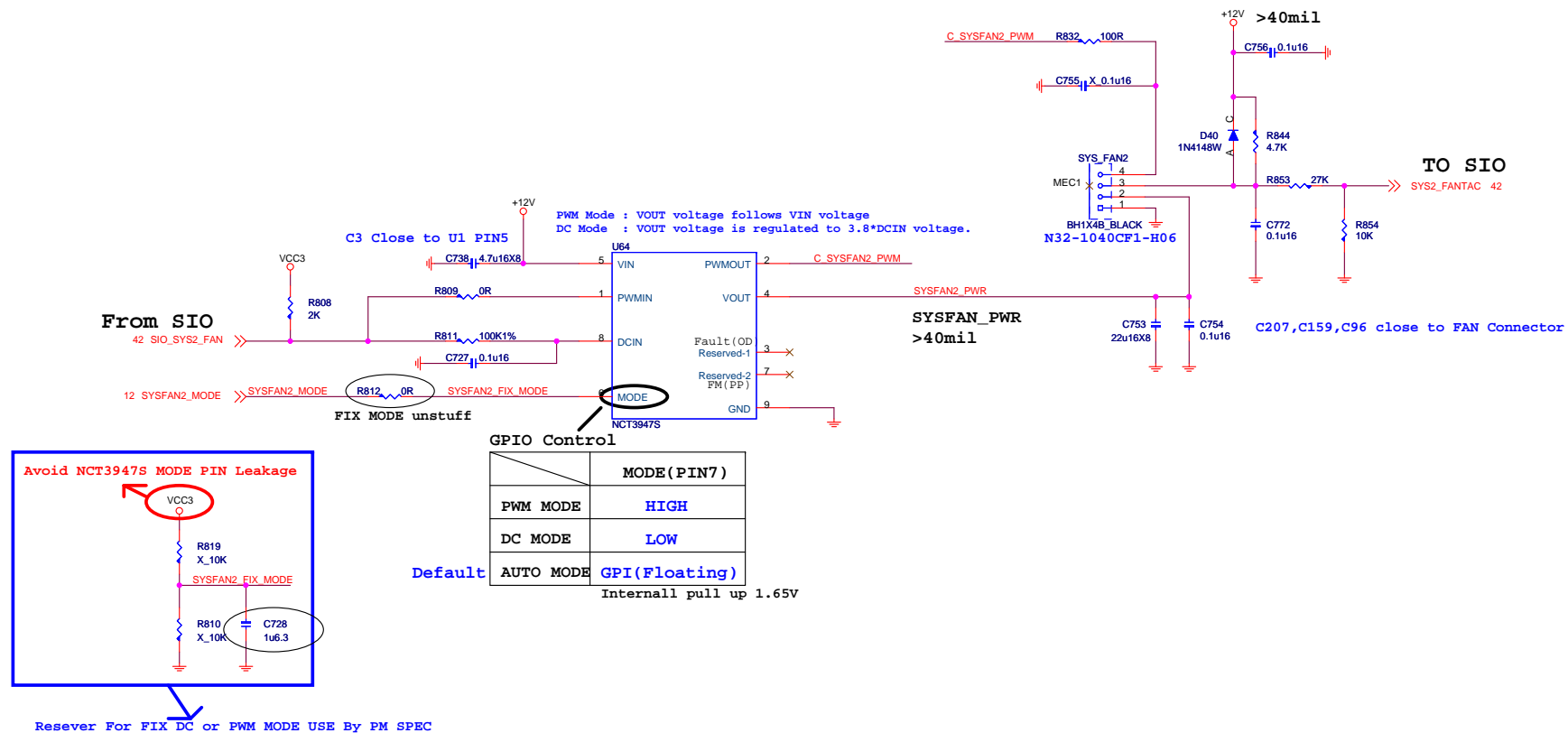
# TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

## 2.GPIO可以由BIOS切换 PWM/DC MODE



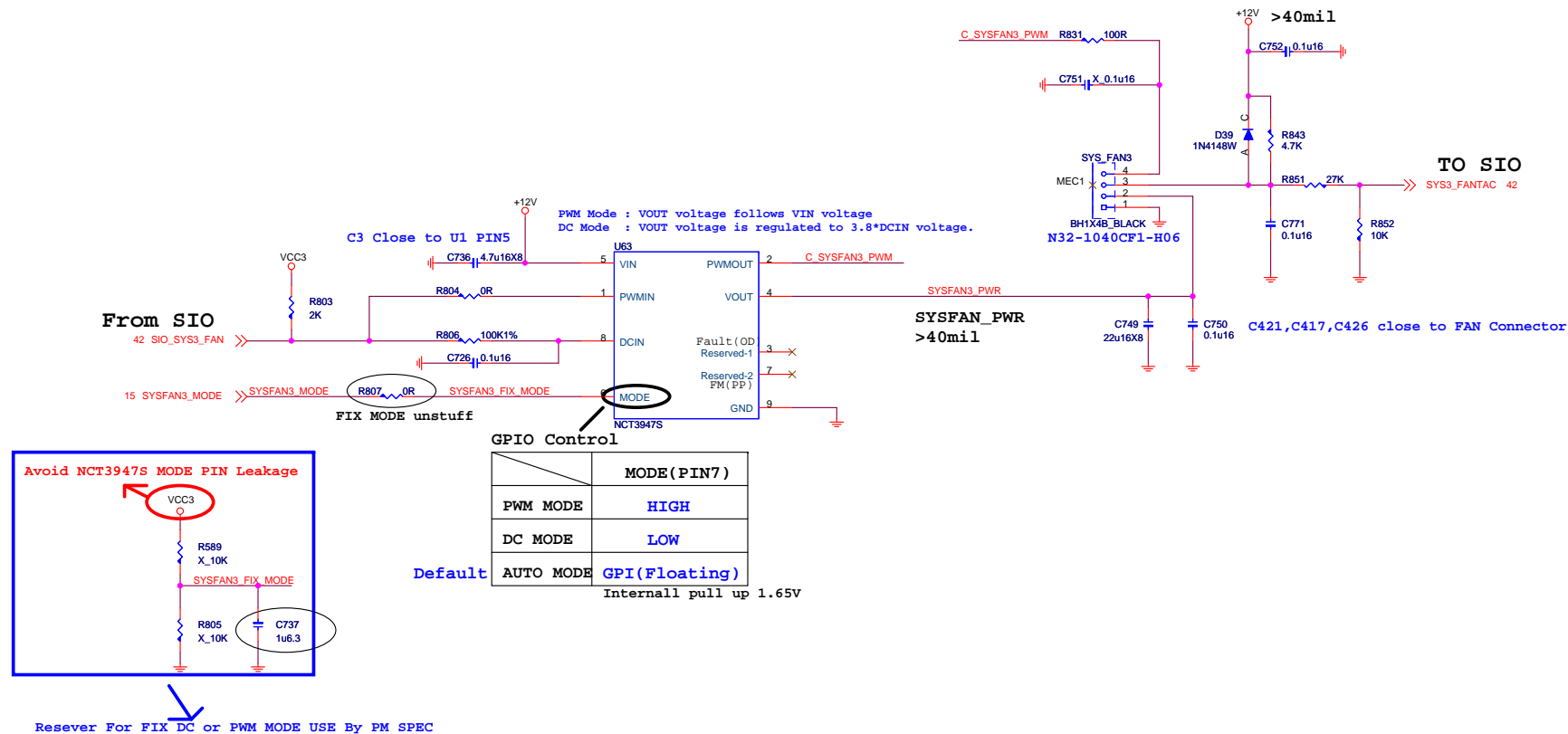
# TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO可以由BIOS切换 PWM/DC MODE

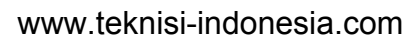


# TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

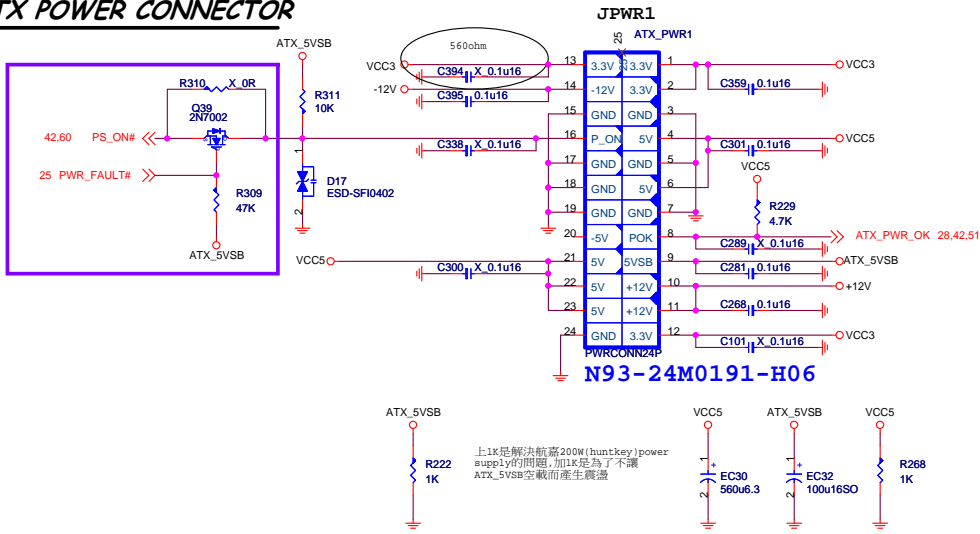
## 2.GPIO可以由BIOS切换 PWM/DC MODE



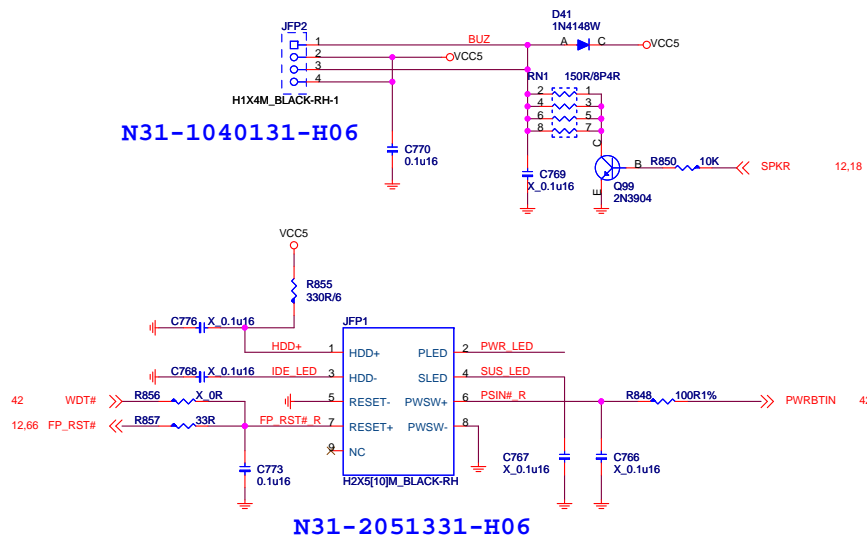
## 2.GPIO可以由BIOS切換 PWM/DC MODE



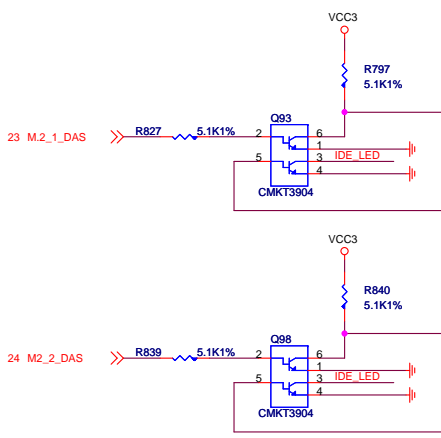
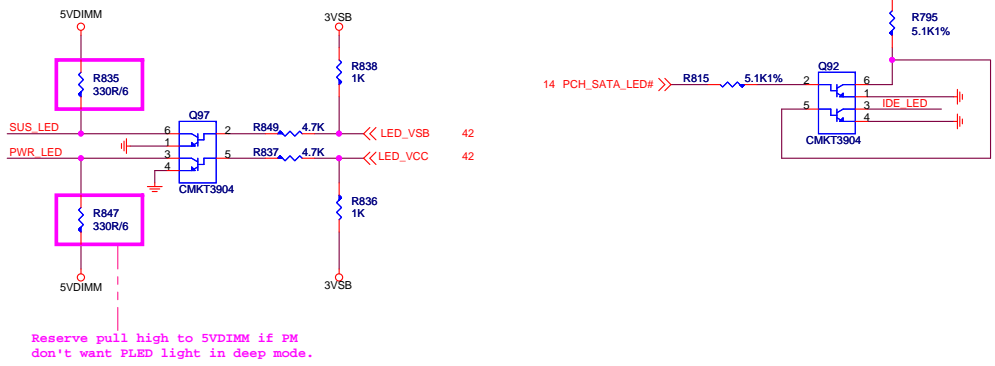
ATX POWER CONNECTOR



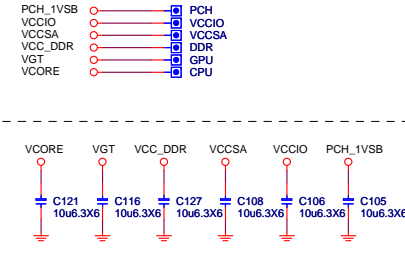
Front Panel



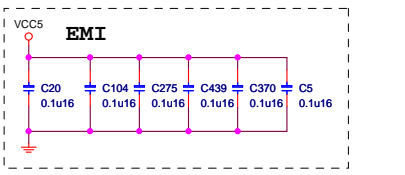
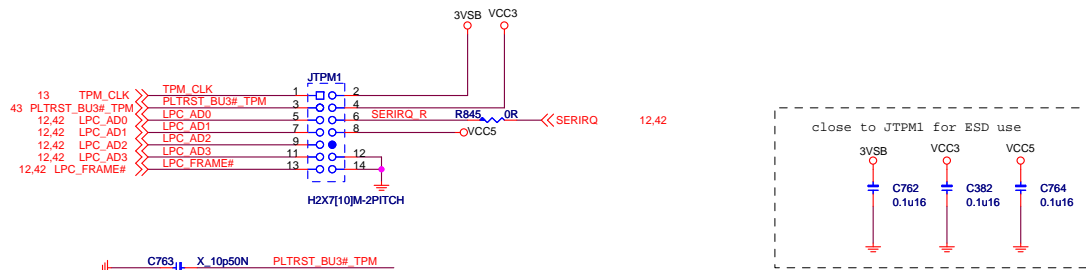
LED



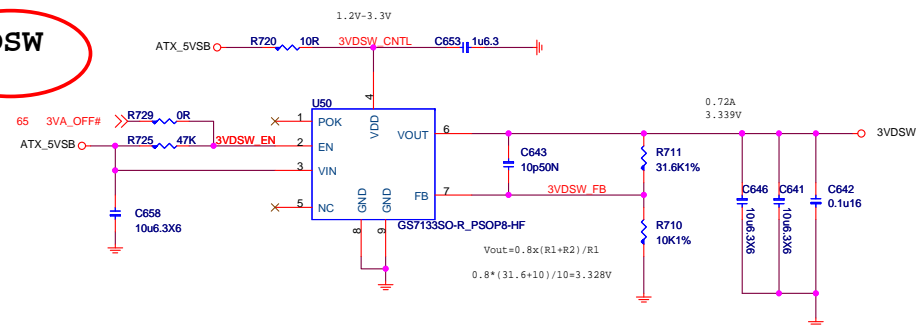
Voltage test point



TPM

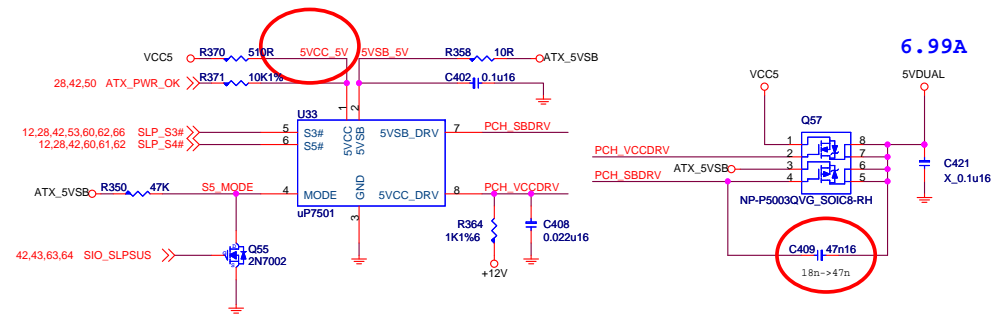


## 3VDSW

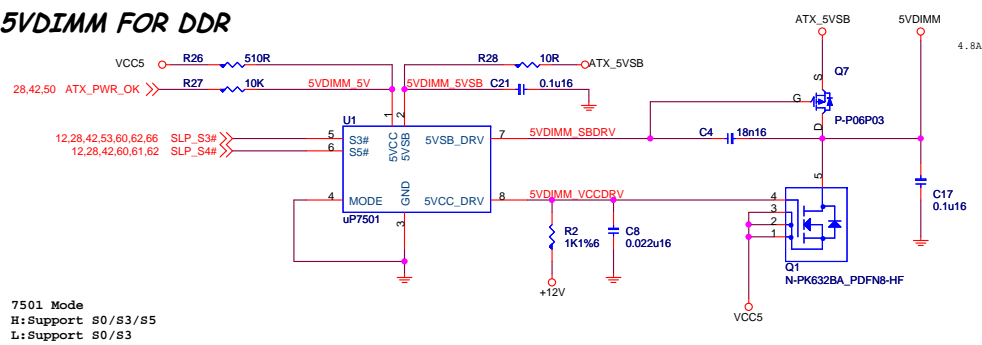


## 5VDUAL

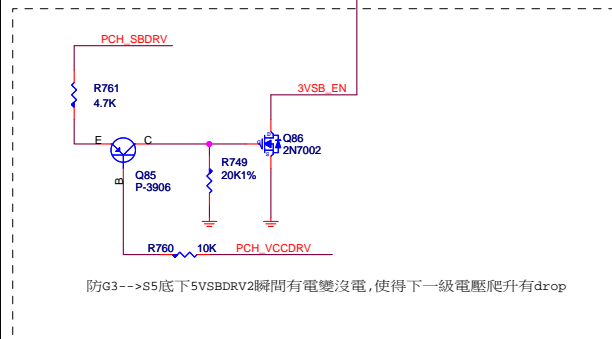
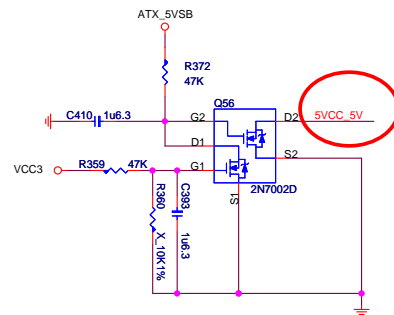
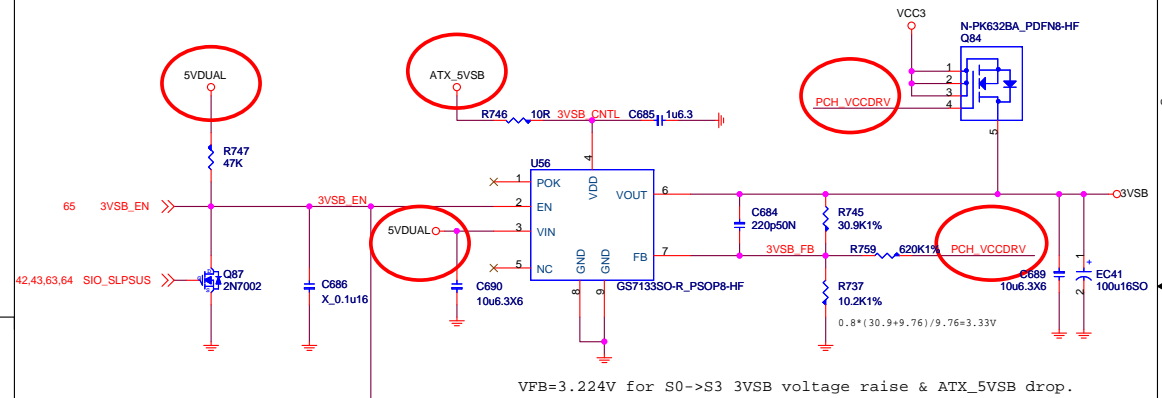
5VDUAL is power source of 1P0SB



## 5VDIMM FOR DDR



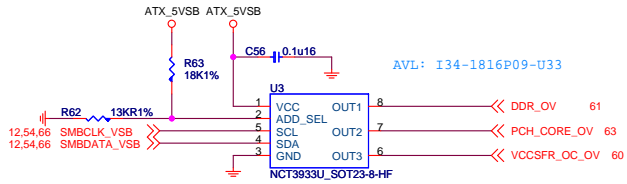
## 3VSB cost down



防G3-->S5底下5VSBDRV2瞬間有電變沒電,使得下一級電壓爬升有drop

UPI VOLTAGE CONSOLE

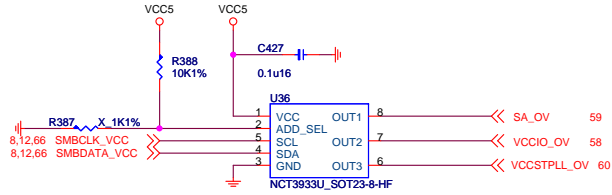
0x26:RH=18K,RL=1.3K



VCC\_DDR  
PCH\_1VSB  
VCCSFR\_OC

UPI VOLTAGE CONSOLE

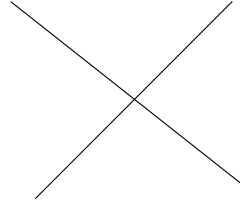
0x20:RH=10K,RL=OPEN



VCCSA  
VCCIO  
VCCST

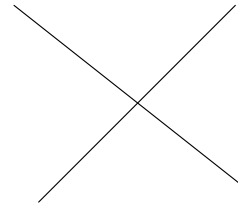
UPI VOLTAGE CONSOLE

0x28:RH=9.1K,RL=3K



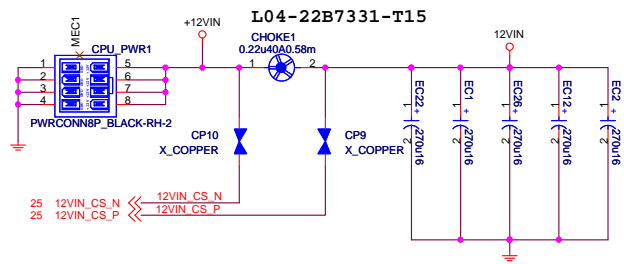
UPI VOLTAGE CONSOLE

0x2A:RH=Open,RL=10K

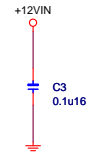


ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%



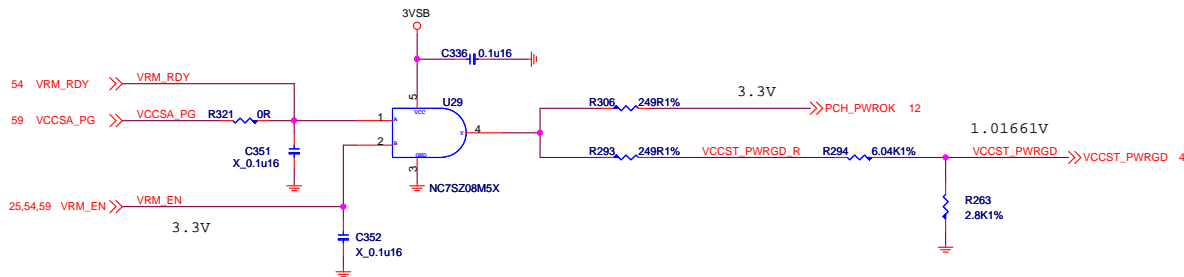


Close to JPWR2

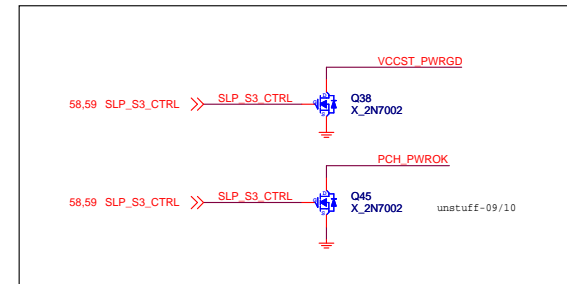
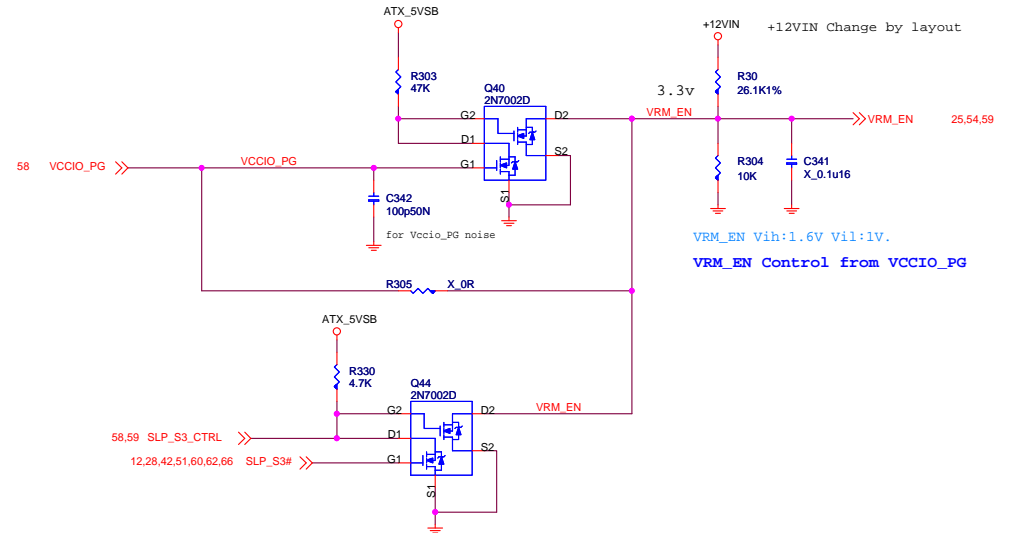


Tripple=30.95A  
VCORE 18.101A  
VGT 8.457A  
VCCSA 4.392A

PCH\_PWROK Control from VCCIO\_PG&VCCSA  
VCCST\_PWRGD Control from VRM\_PGD  
VCCSA&Vcore use same PWM IC, pull up VCC3  
VCCSA&Vcore use different PWM IC, pull up VCCSA  
VCCST\_PWRGD can assert before or equal to PCH\_PWROK, but must never lag it.



VRM\_EN Control from VCCIO\_PG

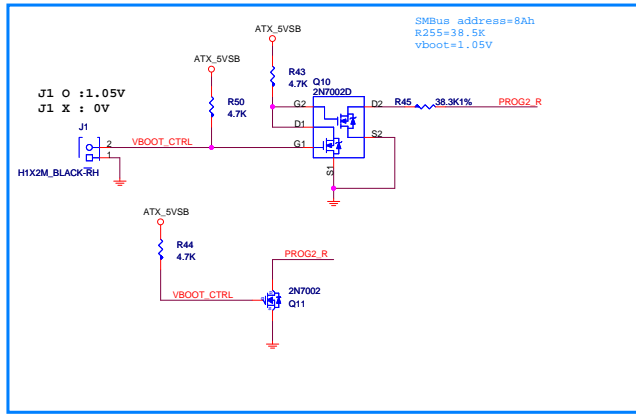
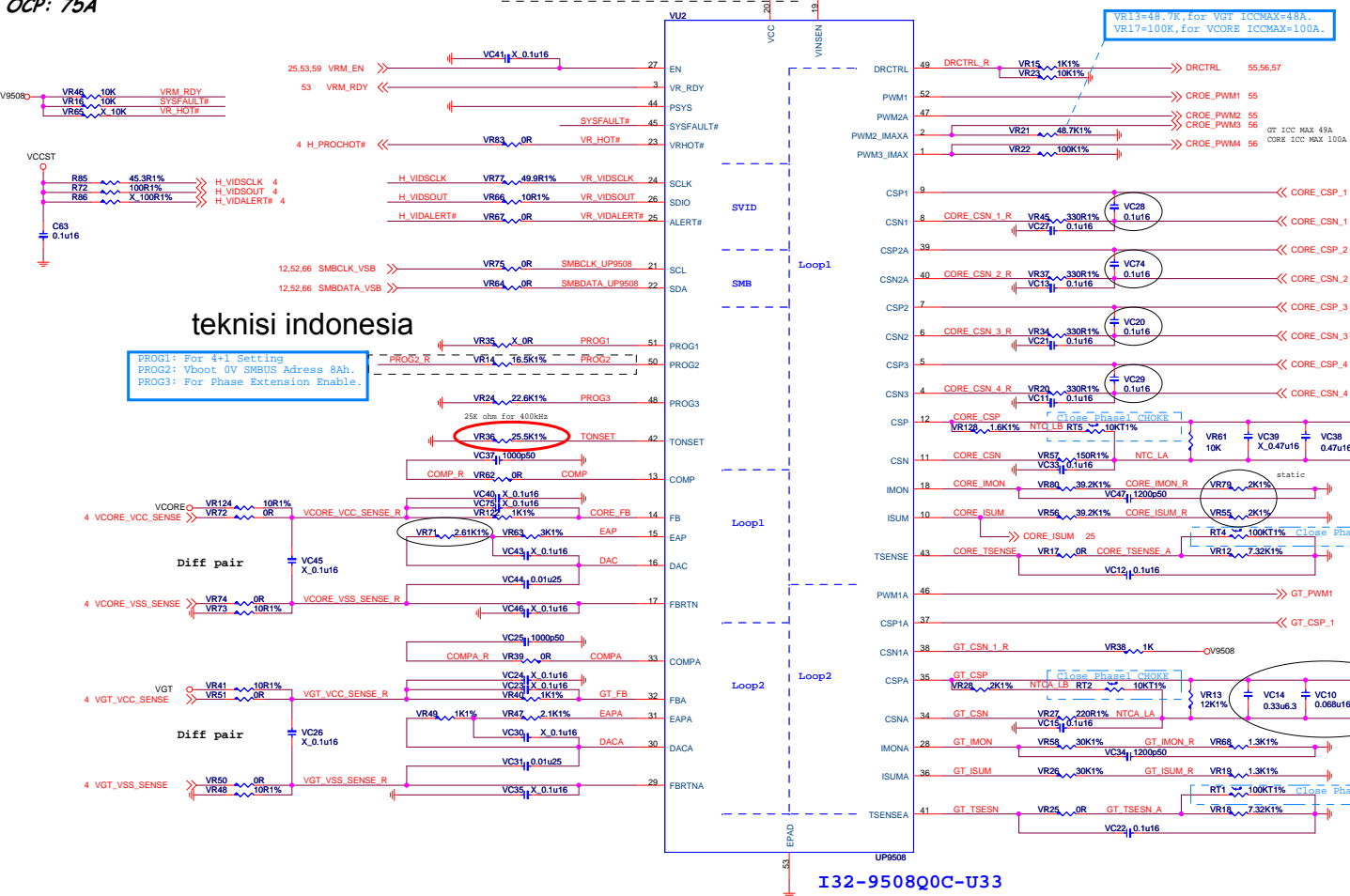


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MS-7A62

Size	Document Description	Rev
Custom	PWM/VRM/Sequence	1.0
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Vcore: ICC Max 100A  
LL: 2.1 mohm  
OCP: 200A  
VGT: ICC Max 48A  
LL: 3.1 mohm  
OCP: 75A



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PROG1: For 4+1 Setting  
PROG2: Vboot 0V SMBUS Address 8Ah.  
PROG3: For Phase Extension Enable.

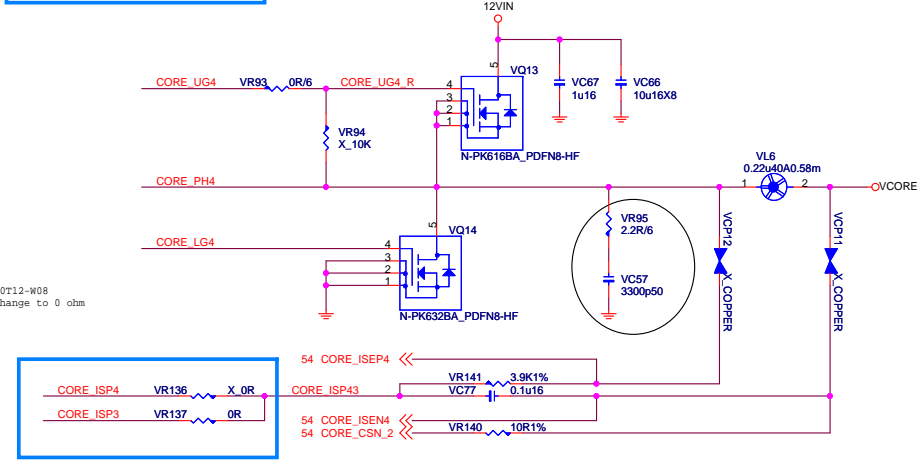
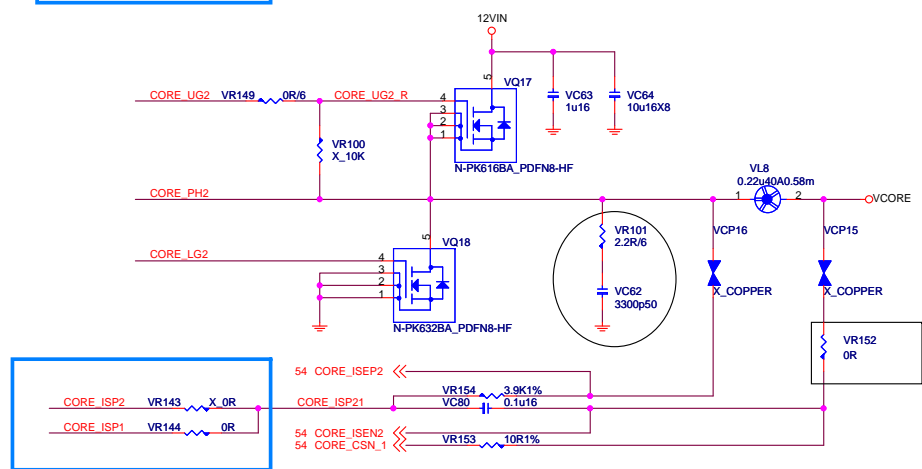
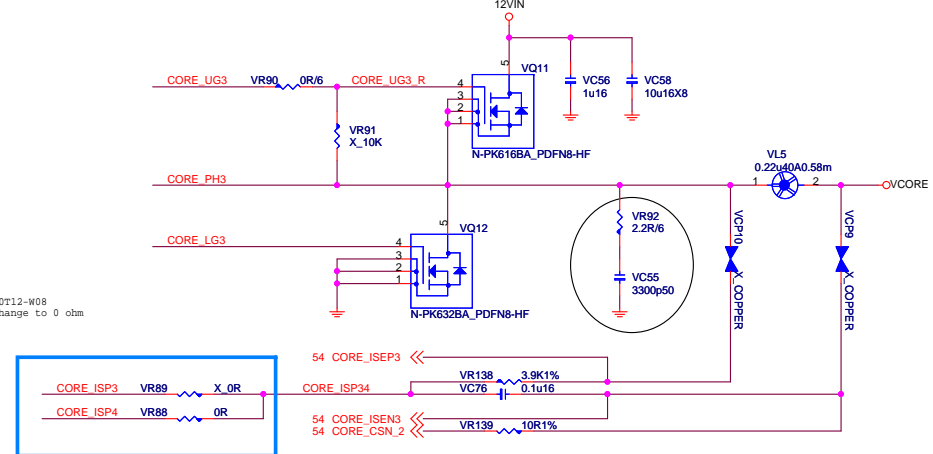
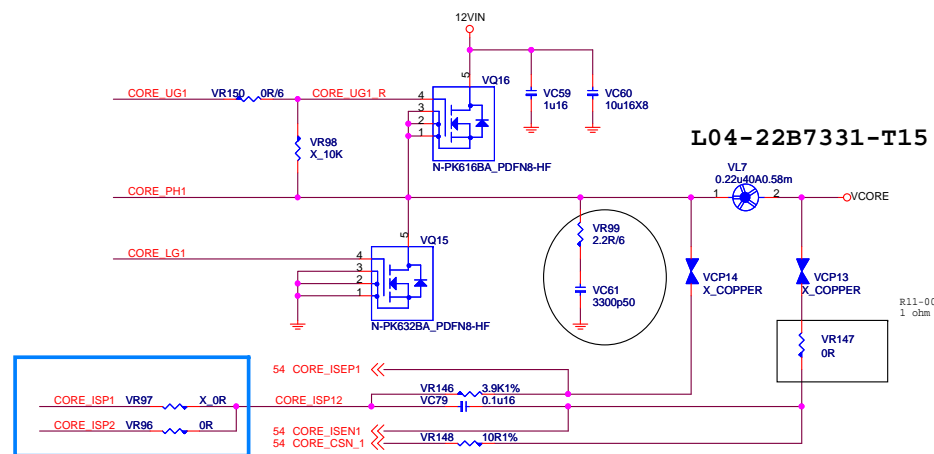
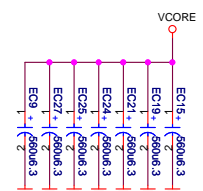
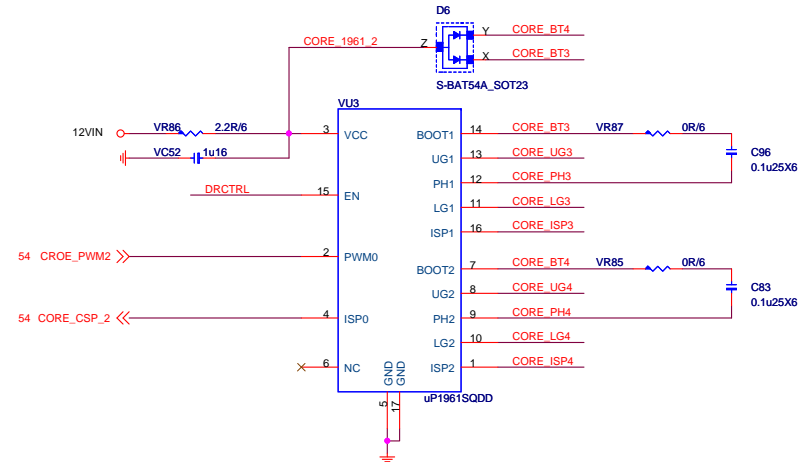
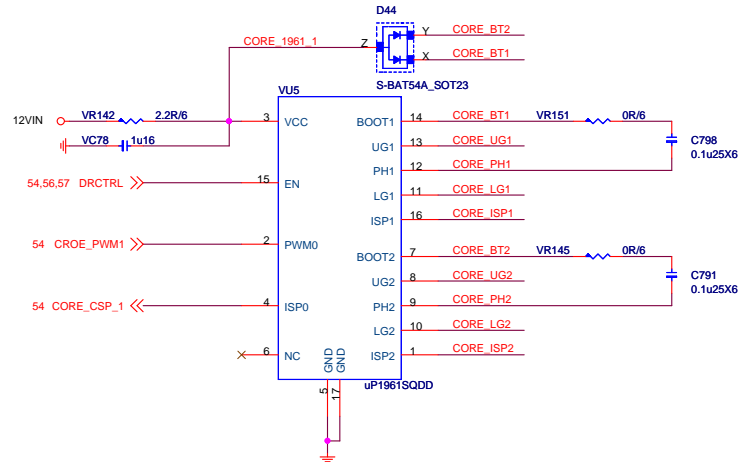
I32-9508Q0C-U33

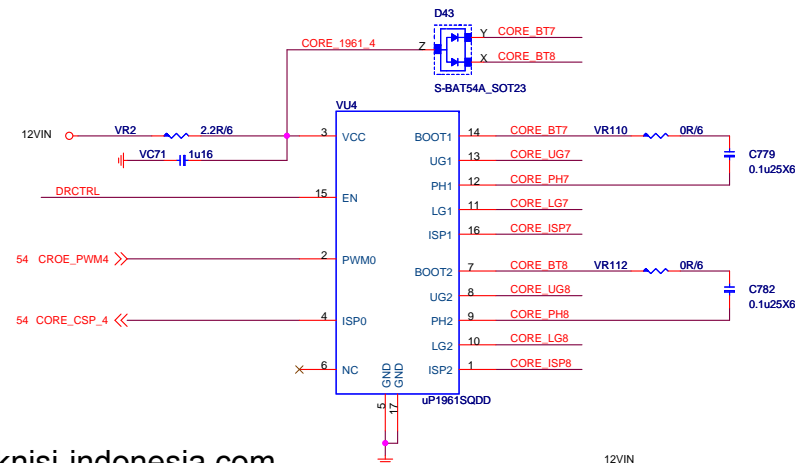
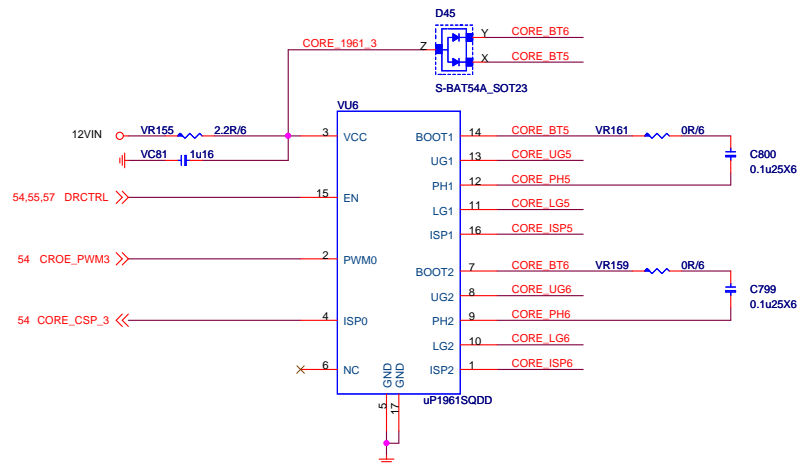


MICRO-STAR INT'L CO.,LTD

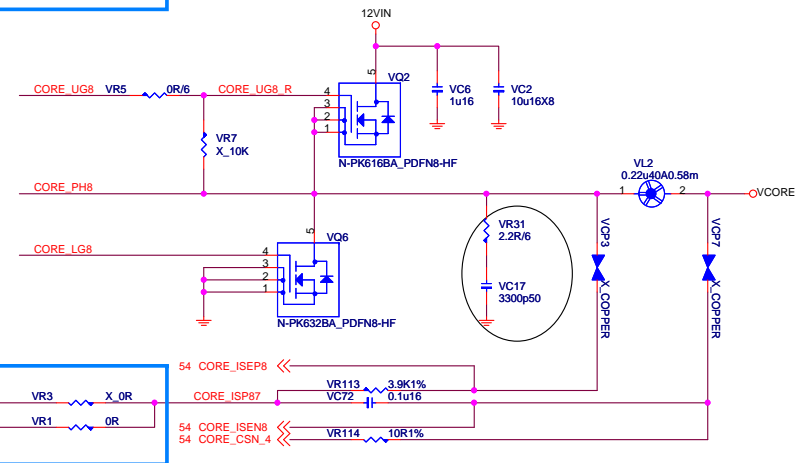
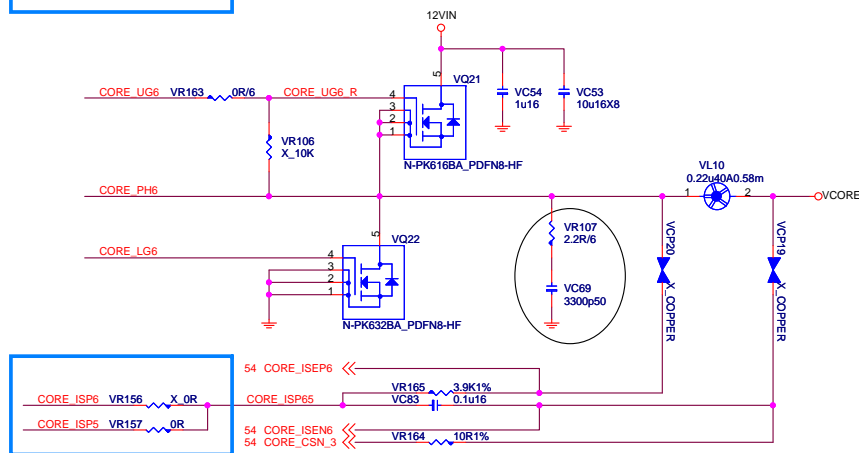
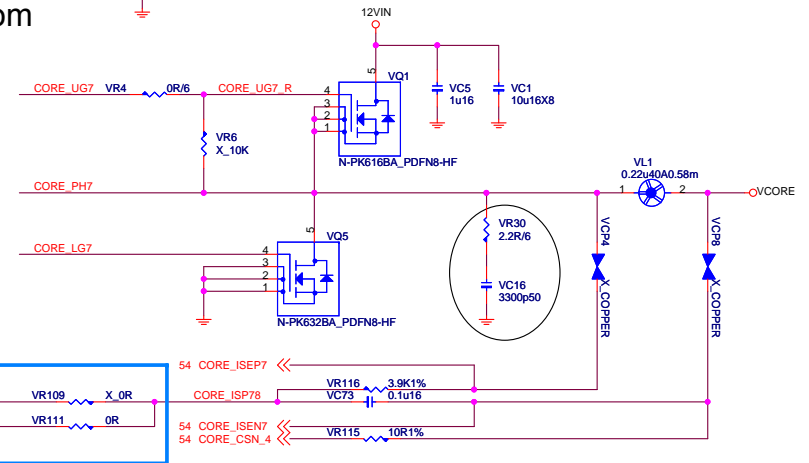
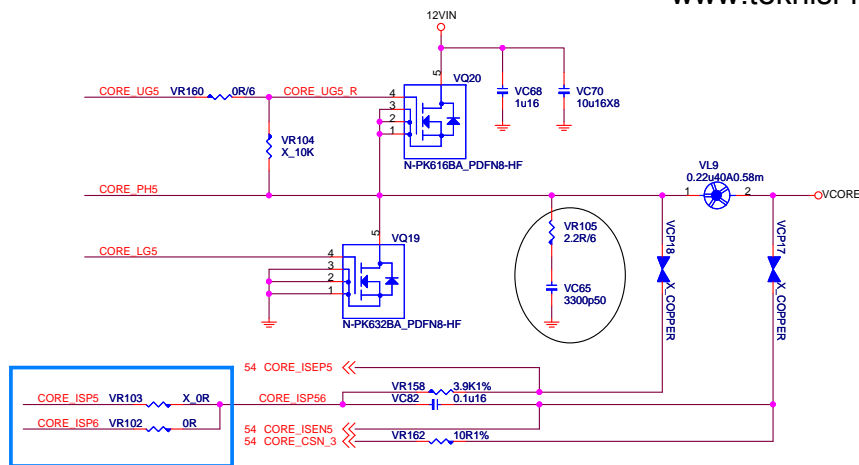
MS-7A62

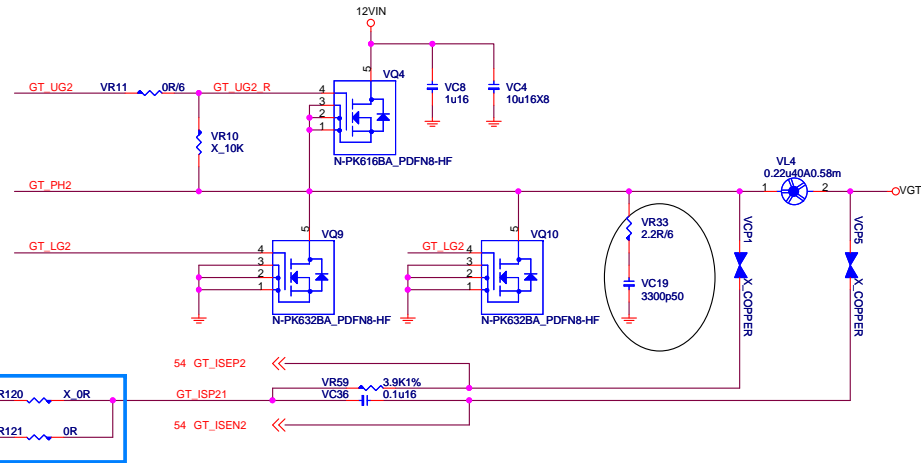
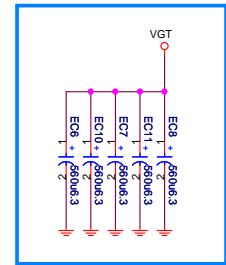
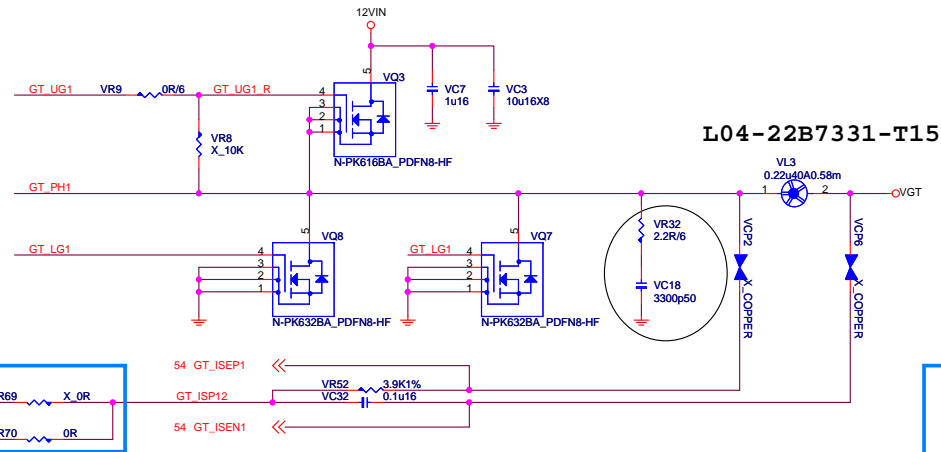
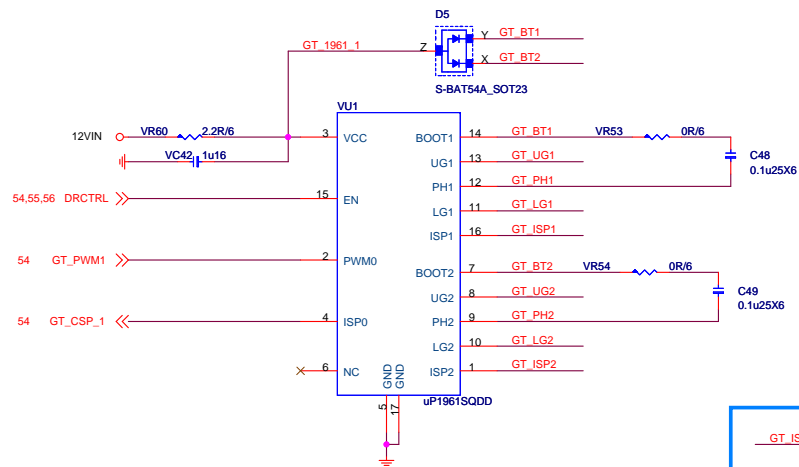
Size	Document Description	Rev
Custom	FWM-UP9508 Vcore+VGT	1.0
Date: Friday, October 14, 2016 Sheet 54 of 71		





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# VCCIO

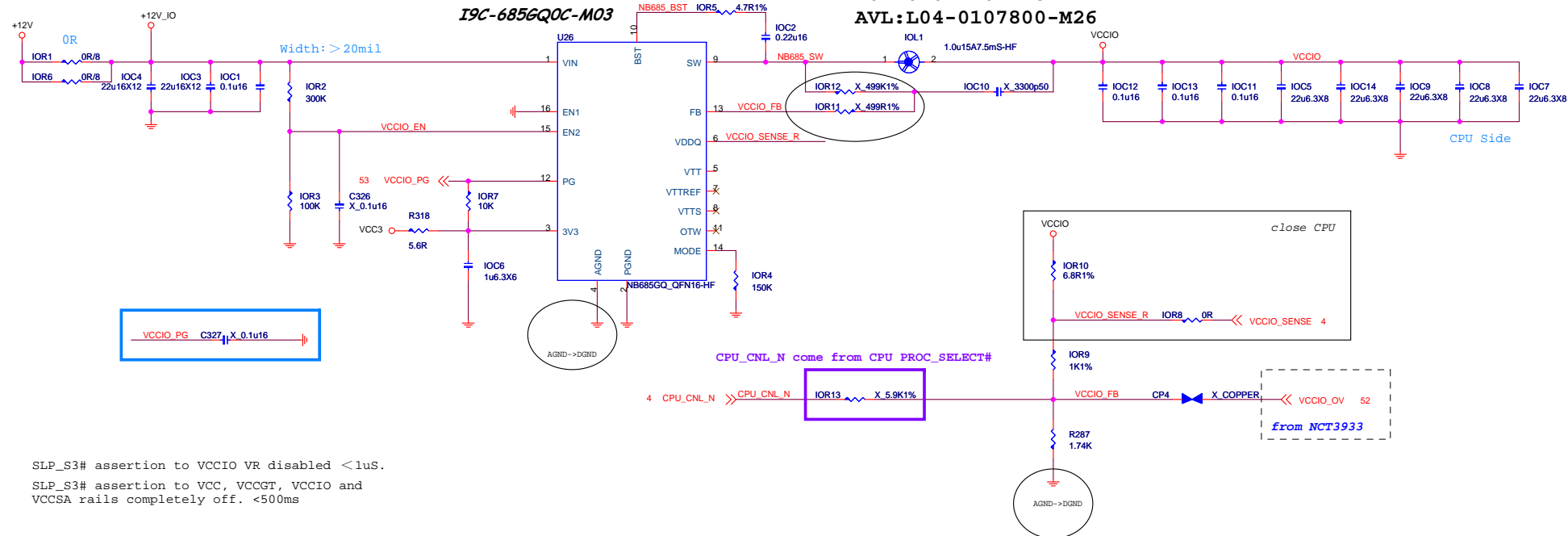
0.95V; 5.5A

support OV=>NB685

IMAX 10A  
ILIMIT=10A~12A  
IOC=ILIMIT+40%\*IMAX/2=12A~14A.

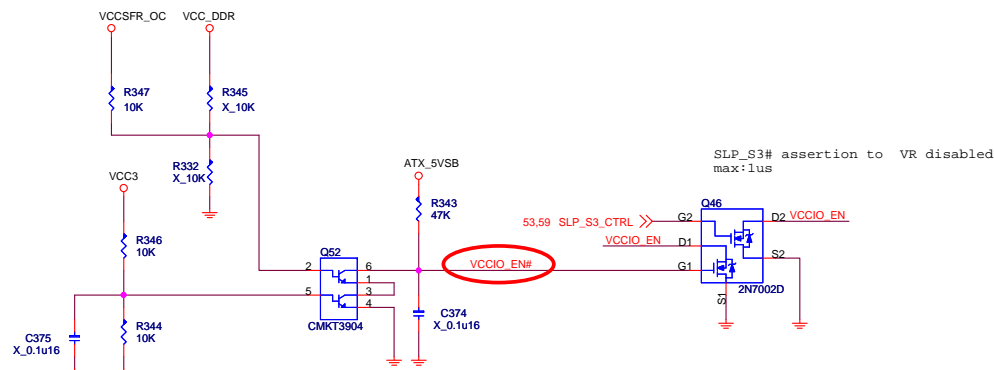
0.7776uH=L=1.1664uH

L04-01072H0-T15  
AVL:L04-0107800-M26



SLP\_S3# assertion to VCCIO VR disabled <1uS.

SLP\_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off. <500ms



# SA Power:1.05V,11.1A

$$OCP = 11.1A * 1.4 = 15.54A$$

$$Rocs(R417) = OCP * R_{dson}(Low\ side) [3.4mohm] / 10uA$$

$$= 15.54 * (3.4mohm / 10uA)$$

$$= 5.2836Kohm$$

Rocs: 5.2836K, OCP:

D03-4C05N03-005 : 15.76A

D03-632BA0C-N03 : 16.24A

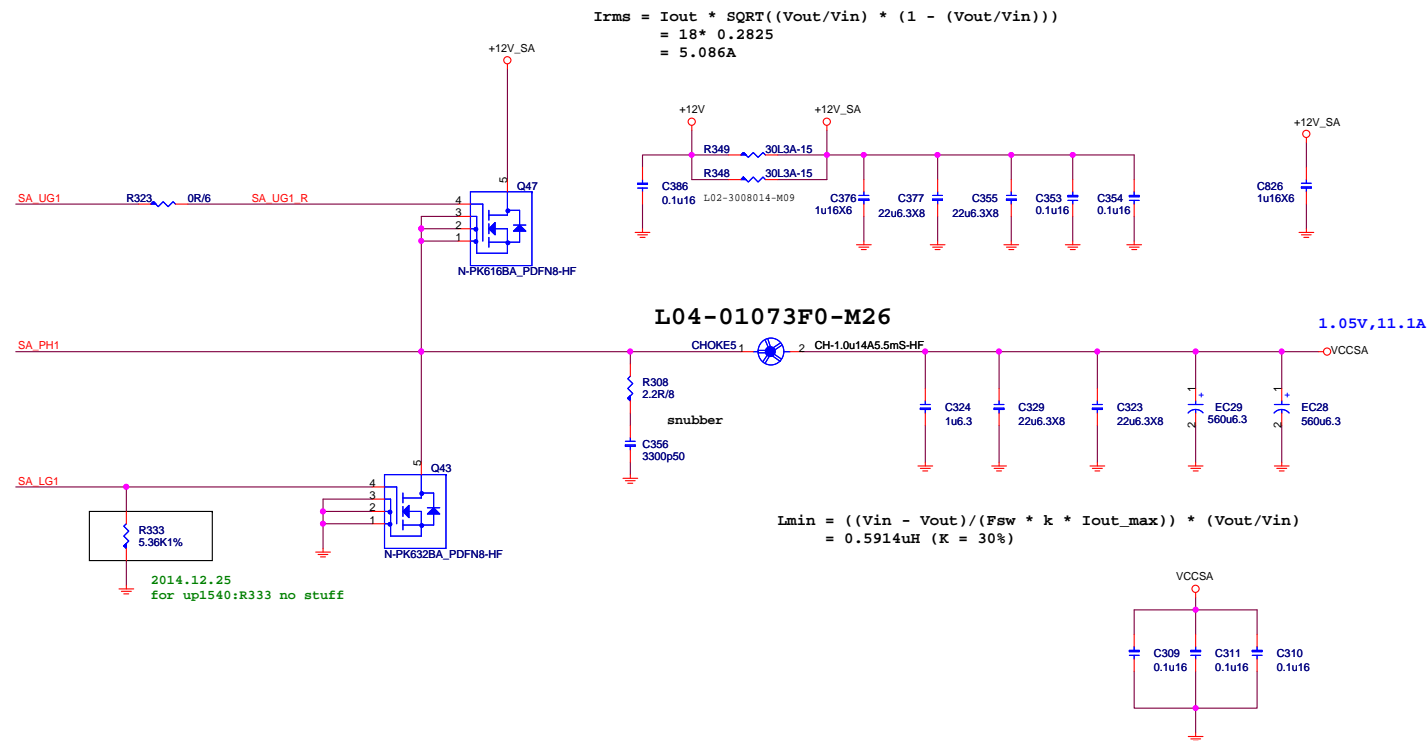
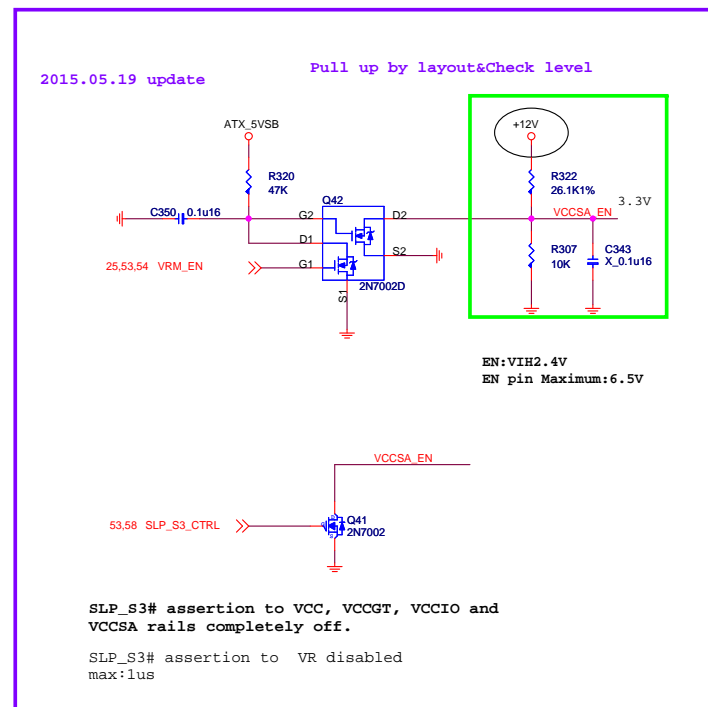
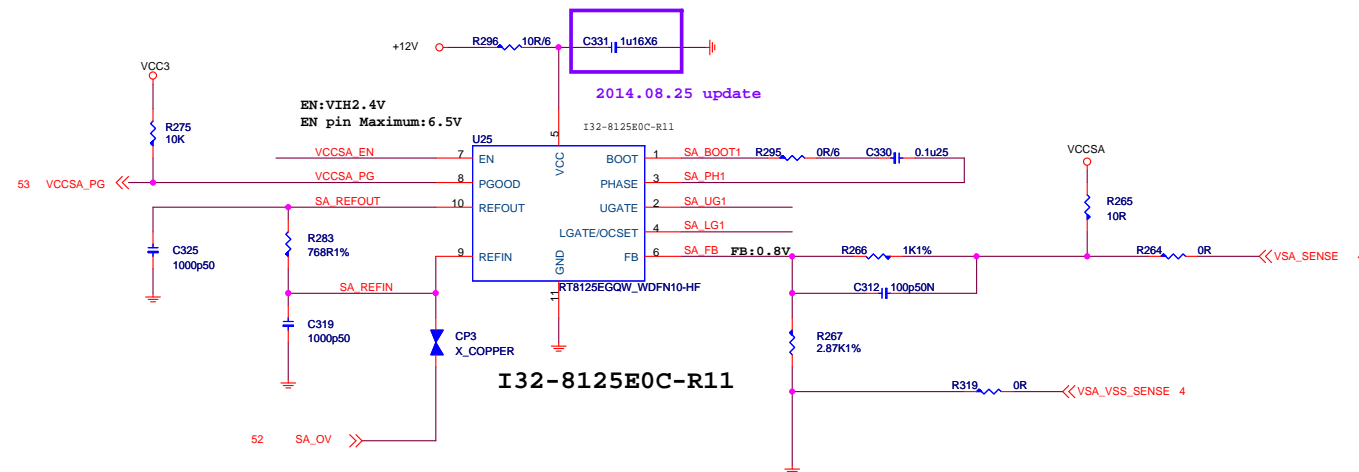
use UBIQ MOS need Check

Rdson (low) 10V

D03-4C05N03-005 : 3.4mohm

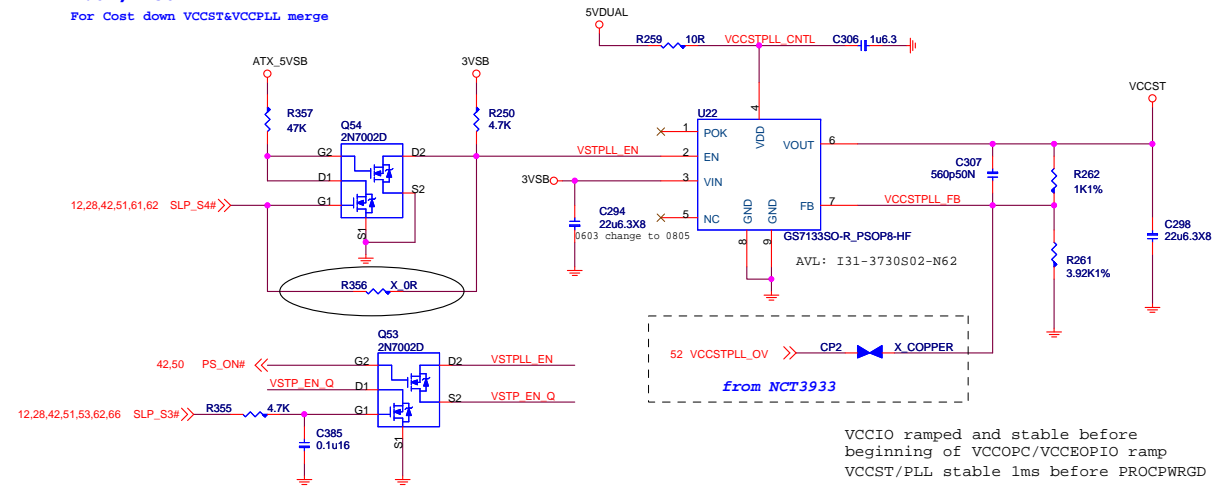
D03-632BA0C-N03 : 3.3mohm

D03-3056M00-U47 : 4.2mohm



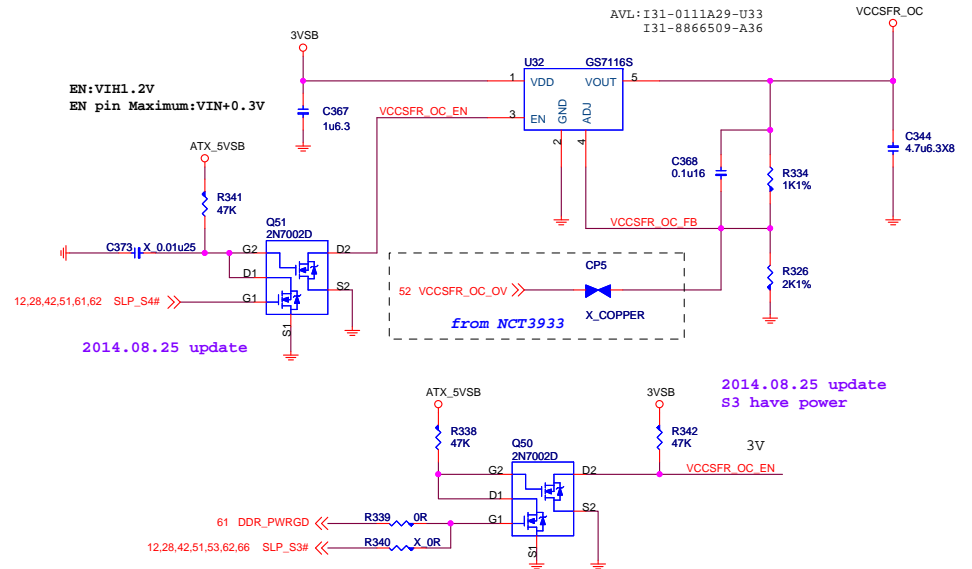
*for Gaming3/5, Classic, ECO and H110*

For Cost down VCCST&VCCPLL merge



2014.08.21 update

1.2V; 110mA



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MS-7A62

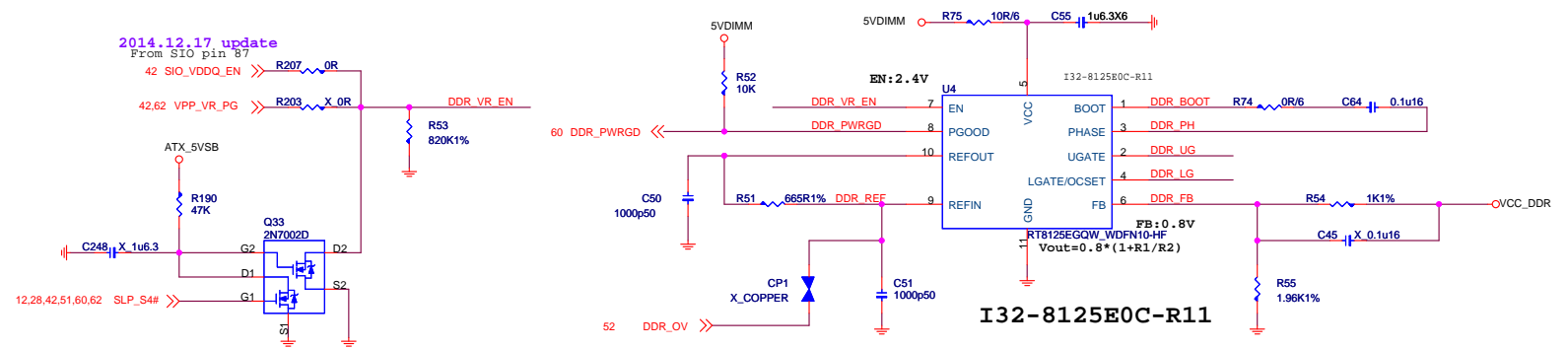
Size Custom	Document Description <b>CPU PWR_ST/PLL</b>	Rev 1.0
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2.5A FOR CPU  
9.5A FOR 4DIMM  
1.2A FOR DDR VTT

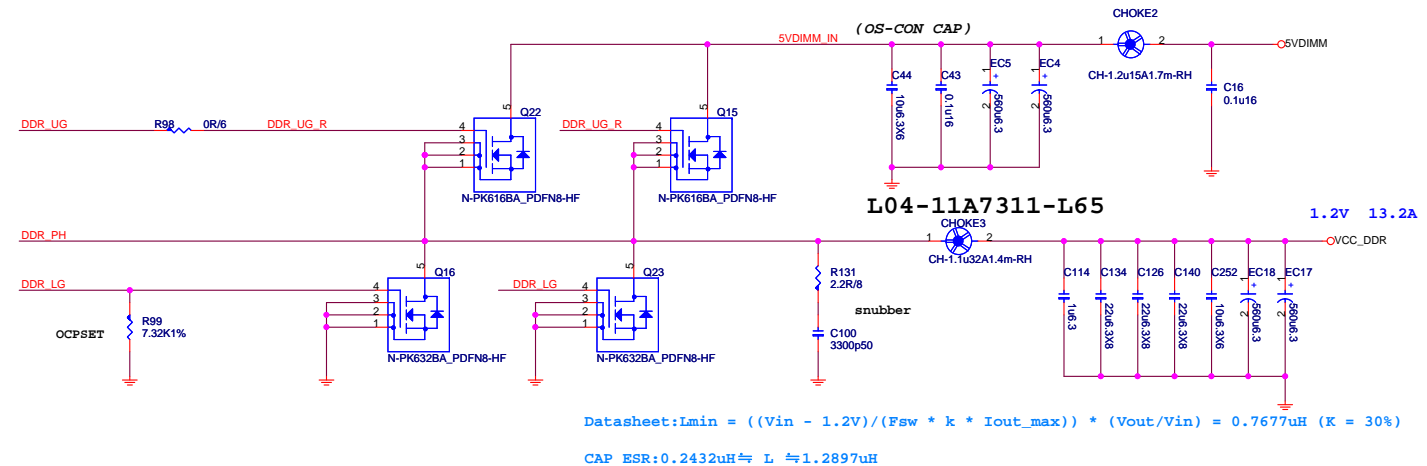
$$\begin{aligned} OCP &= 13.2A * 1.5 = 19.8A \\ R_{ocs}(R3) &= OCP * R_{ds(on)}[(Low\ side)/2]/10uA \\ &= 19.8A * (4.6/2)mohm/10uA \\ &= 4.95Kohm < 5K\ ohm \\ R_{ocpset} &= 7.32K \\ OCP &= R_{ocpset} * R_{ds(on)}(Low\ side)/10uA \\ &= 7.32K * 3.6mohm/10uA \\ &= 20.3A \end{aligned}$$

```
Rdson(1ow)4.5V
D03-4C05N03-O05 : 5 mohm
D03-632BA0C-N03 : 4.6mohm
D03-3056M00-U47 : 6.2mohm
```



```
Irms = Iout * SQRT{(Vout/Vin) * [1 - (Vout/Vin)]}
      = 13.2 * 0.427
      = 5.636A
```

L04-12A7321-L65



Datasheet:  $L_{min} = ((V_{in} - 1.2V) / (F_{sw} * k * I_{out\_max})) * (V_{out} / V_{in}) = 0.7677\mu H$  (K = 30%)

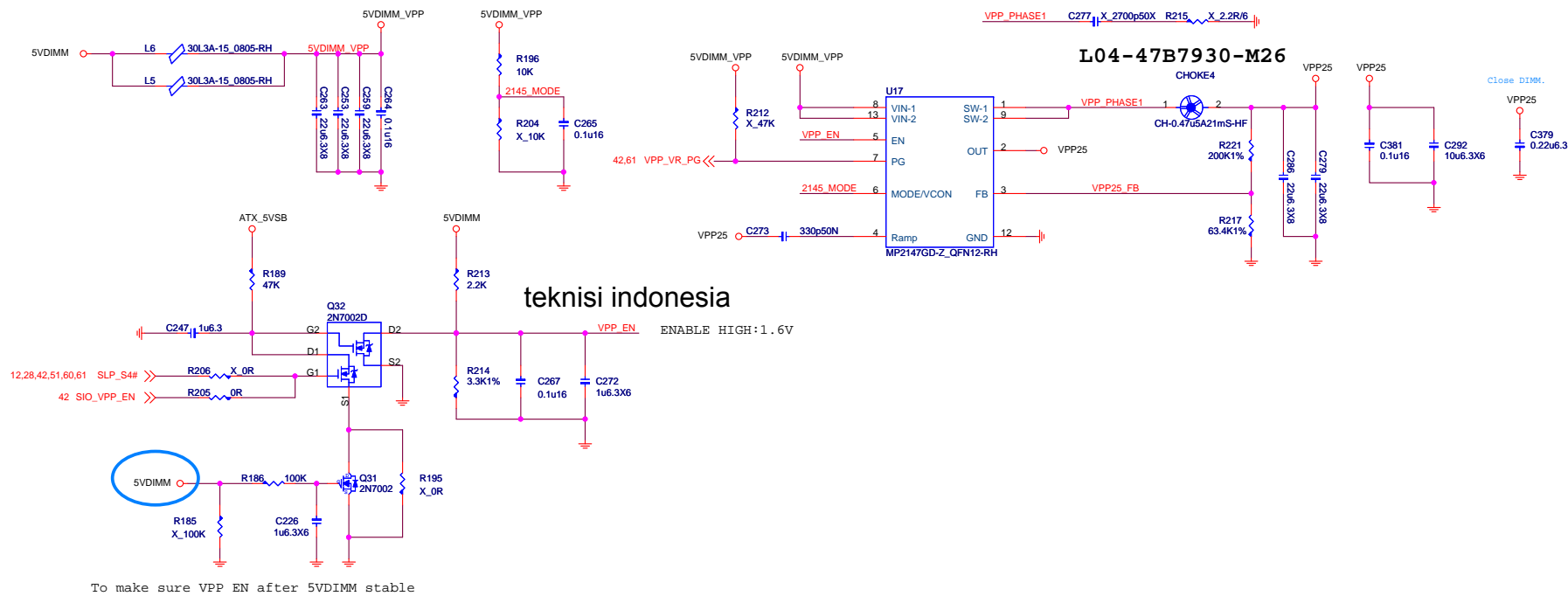
CAP ESR:0.2432uH $\div$  L  $\div$ 1.2897uH

MS-7A62

Size Custom	Document Description <b>DDR4 Power-RT8125C</b>	Rev 1.0
Date: Friday, October 14, 2016		Sheet 61 of 71

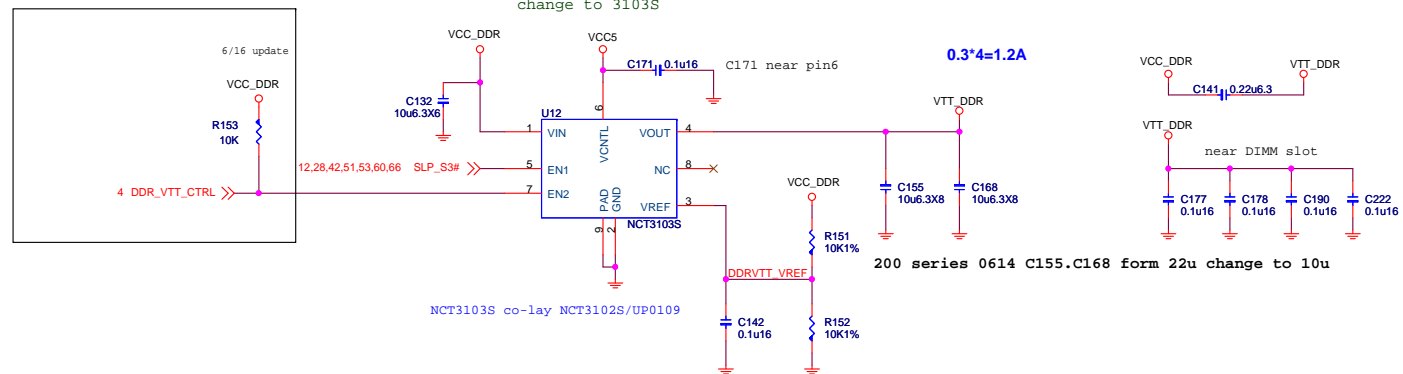
4DIMM :2.84A FOR DDR VPP2.5V

**VPP25 Power**  
**2.5V; 2.24A**



### DDR VTT Power

2015.03.02  
change to 3103S



**MICRO-STAR INT'L CO.,LTD**

MS-7A62

Size Custom	Document Description <b>DDR4 Power-VPP25</b>	Rev 1.0
Date: Friday, October 14, 2016		Sheet 62 of 71

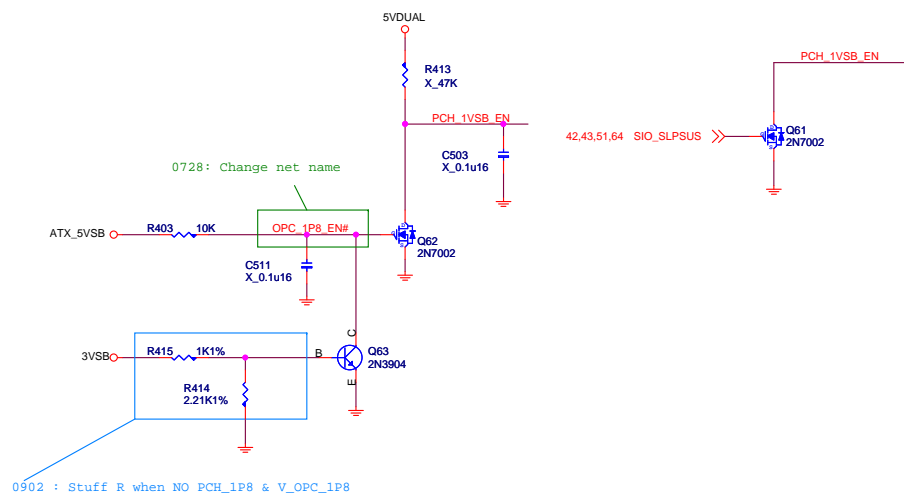
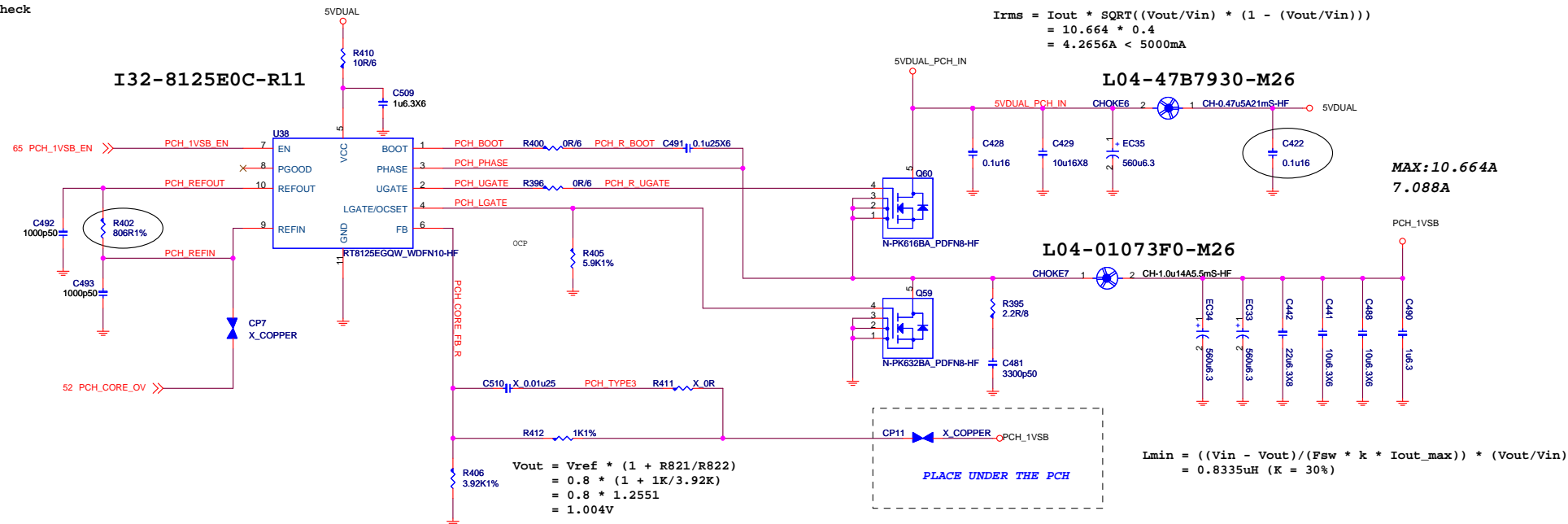
1.0V; 11A

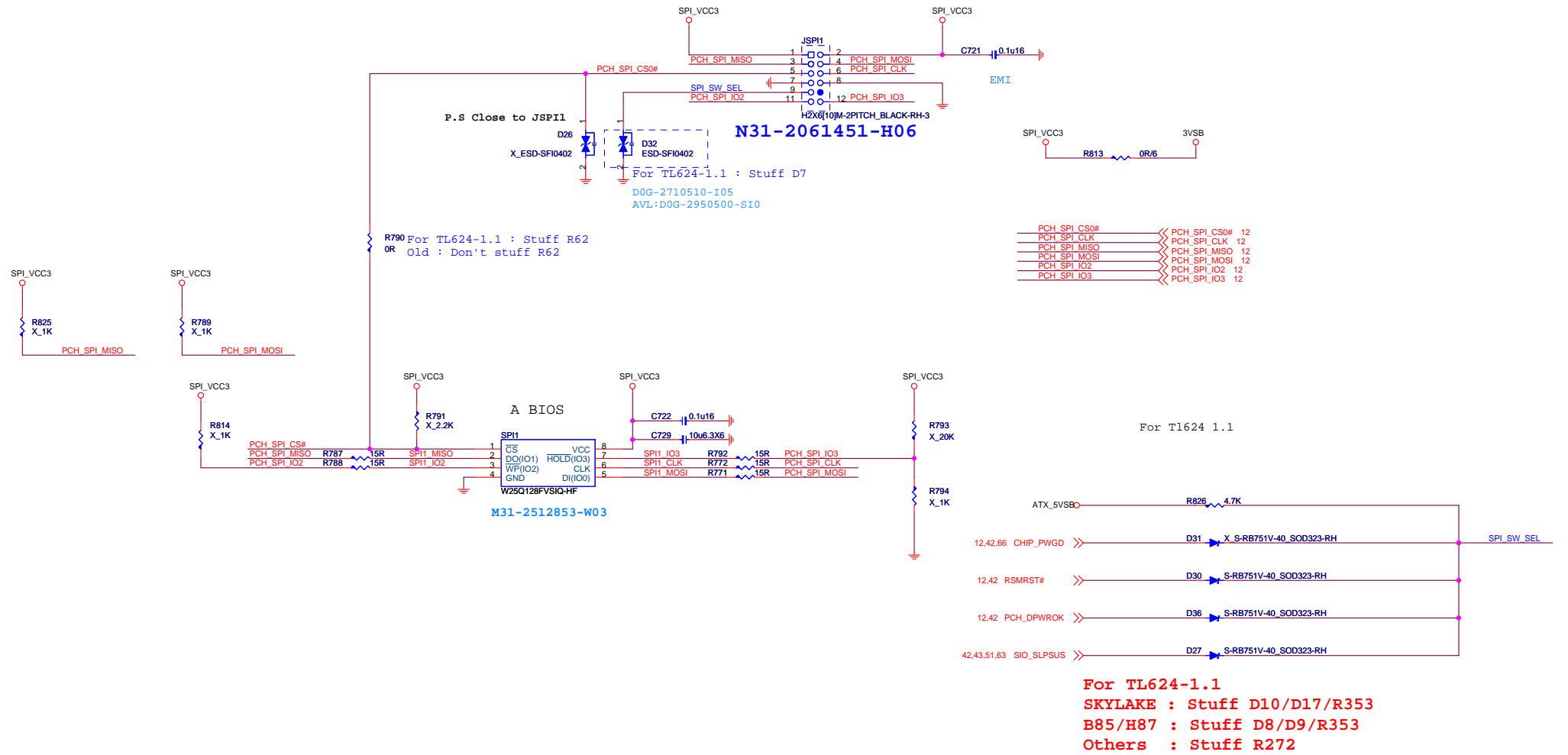
$$\begin{aligned} \text{Rocset} &= 1.5 * \text{Imax} * \text{Rdson(10V)} / \text{Iocset} \\ &= 1.5 * 10.664 * 5\text{mohm} / 10\text{uA} \\ &= 7.998\text{K} \end{aligned}$$

Rocs:7.87K,OCP:  
D03-4C05N03-O05 : 15.74A  
D03-632BA0C-N03 : 17.1A  
use UBIQ MOS need Check

Rdson(10V)4.5V

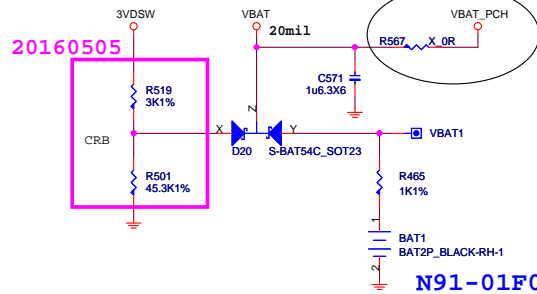
D03-3116M00-U47	: 3.6 mohm
D03-632BA0C-N03	: 4.6mohm
D03-3056M00-U47	: 6.2mohm





# CLR\_CMOS

Co-Lay NOT U12 , Stuff R141



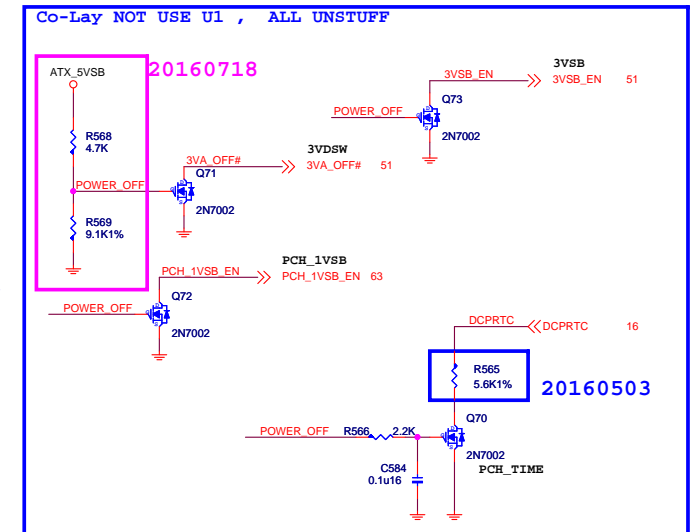
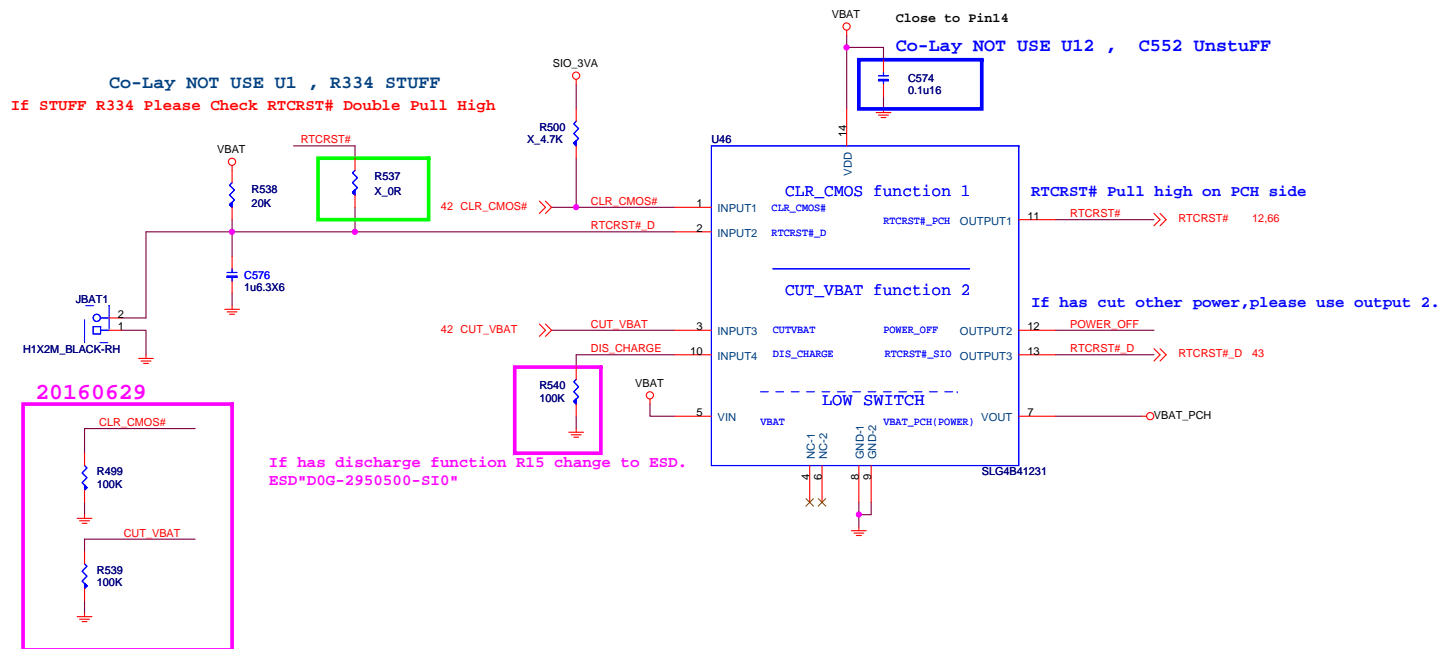
Default

Function 1		
IN		OUT
INPUT1	INPUT2	OUTPUT1
0	1	1
1	0	0
1	1	0
0	0	0

Default

Function 2				
IN		OUT		
INPUT3 & lowswitch EN	INPUT4	OUTPUT2	OUTPUT3	VOUT
0	0	0	1	1
1	0	1	1	0 (discharge)
0	1	1	0	0 (discharge)
1	1	1	0	0 (discharge)

Co-Lay NOT USE U1 , R334 STUFF  
If STUFF R334 Please Check RTCRST# Double Pull High





## PCB



PD0-07A620A-G37  
PD0-07A620A-E48

## HDMI\_LABEL



X\_HDMI LABEL

## AMI\_LABEL



BIOS\_LABEL

## Steel\_Label



Steel\_LABEL1

## Nahimic\_Label



Nahimic\_LABEL1

## MK\_LABEL1



MK\_Z270

## MK\_LABEL2



X\_MK\_H270

## MK\_LABEL3



X\_MK\_B250

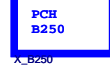
H270:G51-M1SPK20-Q13  
Z270:G51-M1SPK19-Q13  
B250:G51-M1SPK21-Q13

## H270



X\_H270

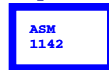
## B250



X\_B250

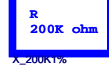
H270:OB1-7A58003-I06  
Z270:OB1-7A58002-I06  
B250:OB1-7A58004-I06

## ASM\_1142



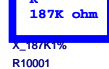
X\_ASM1142

## R10000



X\_200K1%

## R10002



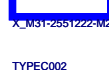
X\_187K1%

## R10001



X\_19.6K1%

## ASPI\_ROOM



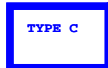
X\_M31-2551222-M24

## HDMI001



X\_N5Y-19M0721-L06

## TYPEC001



X\_N53-08M0591-L06

## TYPEC002



X\_N53-24M0040-L06

## BAT1\_X1

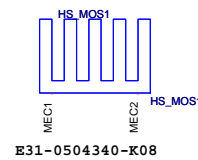
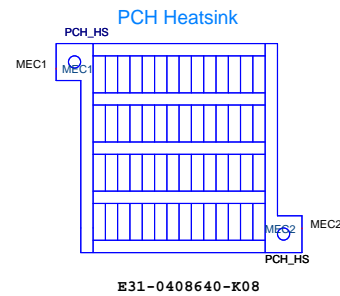


BAT-BCR2032P-RH

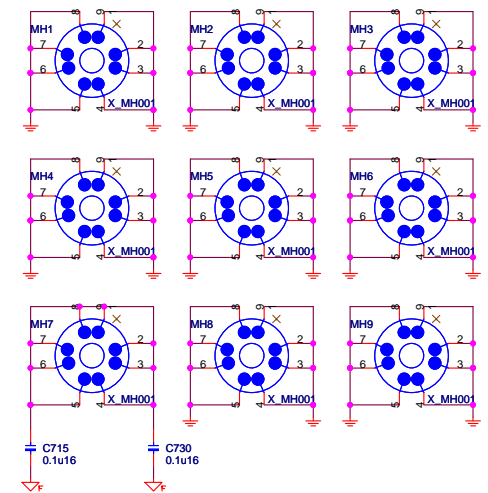
## CPU\_H1



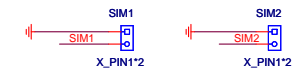
CPU\_H1



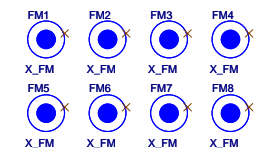
## Mounting Holes



## Simulation



## Optical Fiducial Marks-120



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